
The SPARC™ Solutions Company

ROSS Technology, Inc., in its commitment to provide leading-edge SPARC™ solutions, offers a full range of hardware products that provide the performance, software compatibility, and upgradeability demanded by our worldwide market. Our design expertise ranges from SPARC microprocessors and motherboards to complete workstations and servers.

Founded in 1988, ROSS has supplied high-performance microprocessors to SPARC systems OEMs such as Sun Microsystems, Fujitsu, Tatung, Axil, and ICL, to name a few. To increase our marketshare, ROSS established a program to provide hyperSPARC™ multiprocessing CPU upgrades to end users of Sun SPARCstation™ 10, 20 and SPARCserver™ 600MP systems. Our success in this new market led to the development of motherboard upgrade kits for SPARCstation 5 systems that enable full multiprocessing performance (up to four CPUs) at a cost far below that of a comparable new system. The commitment, experience and design expertise developed in the areas of multiprocessing, upgradeability and the SPARC architecture have established ROSS as a leader in the SPARC community and have contributed to the outstanding overall success of SPARC systems in the workstation market today.

In keeping with our commitment to provide solutions to the increasing demands of our customers, ROSS recently introduced SPARCplug™ and hyperSTATION™ workstations. Available in several configurations ranging from a plug-in workstation module for a tower PC to full servers, SPARCplug workstations provide SPARCstation™ 20-level performance in a reduced form factor and at a lower cost.

For customers with even greater performance needs, ROSS hyperSTATION workstations and hyperSERVER™ systems extend the state-of-the-art of 32-bit multiprocessing to new levels and offer an extensive upgrade path to satisfy future requirements.

All ROSS products are completely SPARC-compliant, run under SunOS (4.1.x) and Solaris (2.x) and are fully compatible with the 10,000+ existing SPARC applications on the market today. ROSS understands its customers' needs and is continually striving to provide the most advanced technology solutions at compelling price/performance points.

Market Overview

Sales of workstations and PCs have grown rapidly in the past few years as the cost of the machines has dropped while the power and functionality have increased. Also fueling this growth has been the proliferation of graphically-oriented operating systems, such as Microsoft's Windows™ and Sun Microsystems' Solaris, and advanced, user-friendly application software capable of running on desktop machines.

Until the late 1980s, microprocessors for PCs and workstations were based on the same architecture, called "complex instruction set computing" (CISC). Modeled after the architecture used for mainframe and minicomputer CPUs, CISC architecture utilizes a larger number of complex instructions to perform internal operations. Very large scale integration (VLSI) technology has enabled increasingly large and complex instruction sets to be performed by a single microprocessor. Most of the PCs sold today contain CISC microprocessors. The principal CISC microprocessor architectures include the x86 architecture pioneered by Intel and used in IBM and IBM-compatible PCs, and the 680xx architecture developed by Motorola and used in Apple's Macintosh system.

In 1987 Sun Microsystems introduced a commercially successful workstation based on an alternative microprocessor architecture called "reduced instruction set computing," or "RISC." RISC architecture utilizes a relatively small number of simplified instructions, all of fixed length, to perform internal operations. By contrast, CISC architectures employ a larger number of more complex instructions of variable length. RISC's design innovations enable RISC microprocessors to achieve higher performance than CISC microprocessors in standard industry benchmarks, especially in floating-point performance. RISC-based workstations have been widely accepted by scientists and engineers, and are increasingly used by businesses for mission-critical and computationally-intensive applications such as financial analysis, manufacturing and inventory management, and relational database management. According to the market research firm International Data Corporation (IDC), worldwide sales of RISC-based workstations and servers increased from 381,000 units in 1990 to 742,000 units in 1994, a compound annual growth rate of 18 percent.

Various RISC architectures have been adopted by the manufacturers of workstations and workstation servers. The varieties include SPARC (Scalable Processor Architecture), first developed by Sun Microsystems; Silicon Graphics' MIPS; Hewlett-Packard's Precision Architecture (PA-RISC); IBM's RS6000; Digital Equipment's Alpha; and most recently, Power PC, which was jointly developed by IBM, Motorola and Apple. Since 1990, SPARC has held the largest worldwide market share of all RISC architectures. According to IDC, 320,000, or 43 percent, of the 742,000 RISC-based workstations and servers shipped in 1994 incorporated SPARC microprocessors. SPARC's 1994 market share was approximately twice the market share of the next leading RISC architecture. As of the end of 1995, the installed base of SPARC-based workstations and servers approximated 1.5 million units.

The SPARC architecture, along with the Sun's Solaris operating system, has facilitated the migration of multiprocessing to servers and workstations. Multiprocessing, the execution of computer instructions and computations over multiple microprocessors within a single computer system, was historically accomplished by duplicating hardware such as memory and input-output (I/O) subsystems. This form of "distributed memory" processing was expensive and typically found only in mainframes and minicomputers. As SPARC and Solaris have evolved, "shared-memory" multiprocessing has become a significant segment of the server market, and a growing segment of the desktop workstation market.

The Market Opportunity

Since its inception in 1988, ROSS has brought to market four generations of hyperSPARC microprocessors, the first of which included the 40-MHz microprocessors used in the SPARCserver 600 series multiprocessing systems in 1991, launching Sun into the multiprocessing market segment. The company plans to continue utilizing its strengths in design, testing and multiprocessing, as well as its expertise in advanced manufacturing technologies such as multi-die packaging (single integrated circuit packages containing multiple bare semiconductor die connected by advanced substrate technology), to maintain technological leadership in SPARC microprocessor chipsets and modules. Among ROSS' design wins are the inclusion of the 100-MHz hyperSPARC microprocessor in Sun's SPARCstation 20 Model HS11 in 1994, the 125 MHz and the 150 MHz hyperSPARCs in Sun's follow-on products. ROSS has also achieved design wins with OEMs such as PFU (a division of Fujitsu), Auspex, Axil and Fujitsu in their S-family workstations and DS/90 servers.

The company sees a substantial opportunity in several market segments for companies developing high performance microprocessors and associated semiconductor products for SPARC-based computer systems. First, the manufacturers of SPARC-based workstations and servers will continue to represent a strong source of demand for SPARC microprocessors. According to IDC, worldwide sales of SPARC-based workstations and servers increased from 133,000 units in 1990 to 320,000 units in 1994, a 25 percent compound annual growth rate. IDC estimates that total sales of SPARC-based systems exceeded \$5 billion in 1995. ROSS currently serves this market through the sale of stand-alone multi-die packages (MDPs) and microprocessor modules (plug-in "daughtercards" containing MDPs and other components on a small printed circuit board). The company has also developed complementary application specific integrated circuits (ASICs) for this market, completed SPARC-based motherboards which utilize a 66 MHz MBus and developed entire workstations that combine all of these technical innovations into several new high-performance products. ROSS' entry into the workstation market is a logical progression of ROSS' ongoing commitment to provide world-class SPARC solutions to the industry.

Furthermore, the company believes that owners of existing SPARCstation 10 and SPARCstation 20 class workstations and SPARCserver 600 class servers will, in increasing numbers, choose to upgrade the performance of their existing machines by purchasing upgrade modules that incorporate the latest generation of high-speed SPARC microprocessors rather than purchasing a new machine. According to IDC estimates, the installed base of these machines was approximately 283,000 units at the end of 1994. These workstations incorporate a CPU subsystem interface known as the MBus, an open interface standard co-developed by ROSS and Sun. Currently, the majority of these machines are powered by a single 40-, 50-, 60-, or 75 MHz SuperSPARC microprocessor manufactured by Sun Microelectronics (formerly SPARC Technology Business), and, due to the MBus design, each is fully upgradeable and multiprocessing capable. By installation of one of ROSS' single-, dual- or quad-processor hyperSPARC upgrades, which currently run at clock speeds that range from 90 MHz to 180 MHz, the performance of these machines can be increased up to seven times. The prices of the upgrade modules are generally below those of new machines with comparable performance. In addition, users of these machines generally have made a substantially greater investment in SPARC-specific application software licensed to their existing workstations than in their SPARC workstation hardware. For these reasons, ROSS believes these users will increasingly choose to upgrade the performance of their machines with ROSS upgrade modules. Demand for upgrade products will also grow as the installed base of SPARC-based systems grows and as new machines incorporating today's leading-edge SPARC microprocessors become upgrade vehicles in the future.

There is also a substantial installed base of Sun's lower performance non-MBus SPARC workstations and servers (estimated by IDC to be 689,000 units at the end of 1994). These machines incorporate a single dedicated microprocessor mounted directly on the CPU's motherboard. A substantial market exists for replacement motherboards incorporating the latest generation of hyperSPARC microprocessors that upgrade the performance of these machines. In February 1996, ROSS introduced motherboard upgrade kits for Sun SPARCstation 5 machines, adding 236,000 units to the installed base of prospects.

ROSS also sees continued growth in the demand for SPARC microprocessors in non-workstation applications such as telecommunications, data communications and "embedded" (non-computer) applications, presenting additional market opportunities for the company.

Strategy

ROSS strives to be the leading level-playing-field supplier of high-performance microprocessors, workstations and associated semiconductor products based on the SPARC architecture. Our objective is to take advantage of current conditions and trends in the computer and microprocessor industries, including the continued marketshare leadership of the SPARC architecture among all RISC architectures; the desire of OEMs to purchase SPARC microprocessors, microprocessor modules and motherboards from multiple suppliers; the ability of owners of previous generations of SPARC workstations to cost-effectively increase workstation performance by purchasing upgrade modules or motherboards that incorporate the newest generation of high-performance SPARC microprocessors; and the growing use of RISC microprocessors in communications and embedded applications. The key elements of the company's business strategy include:

Maintain Technological Leadership — Improving the performance of its hyperSPARC product family is essential for ROSS to compete effectively in the SPARC marketplace. To this end, ROSS will introduce hyperSPARC microprocessors running at clock rates of 180 MHz in 1996. ROSS will also continue to take full advantage of its expertise in the design and integration of cache memory and control. It will seek to achieve additional performance improvements by increasing the size of the cache memory used in its microprocessor configurations from 256-kilobyte to 512-kilobyte and one-megabyte configurations, and by implementing improvements to the underlying hyperSPARC design.

Diversify Customer Base — Historically, sales have been concentrated among a limited number of large OEM customers. ROSS has entered the upgrade market and made available its hyperSPARC CPU upgrades to the installed base of SPARCstation 10, 20 and SPARCserver 600MP owners. ROSS has further expanded its market to include SPARCstation 5 owners with its motherboard upgrade kits. SPARCplug and hyperSTATION workstations are also now available to customers who need high-performance systems.

Preserve Investment in SPARC Installed Base — The installed base of SPARC workstations and servers represents a substantial growth opportunity for ROSS Technology. The company currently manufactures and markets hyperSPARC upgrade modules for high-end SPARCstation 10 and 20 class workstations and SPARCserver 600 series servers. It has also developed motherboard upgrade kits for Sun's lower-performance SPARCstation 5 workstations. The company expects the market for its upgrade products to grow as future increases in processor performance make today's leading-edge SPARC workstations and servers into tomorrow's upgrade vehicles, and as the aggregate dollar investment in the software designed to run on these machines continues to grow.

Establish and Maintain Strategic Manufacturing Relationships — ROSS has established strategic relationships with semiconductor manufacturers and other suppliers that possess state-of-the-art production facilities and process technologies. Fujitsu, utilizing its 0.4 micron complementary metal oxide semiconductor

(CMOS) process technology, currently manufactures silicon wafers for ROSS. The company is also working with Fujitsu to migrate wafer production to finer circuit geometries, which will increase processor speeds and the number of gross die per wafer. ROSS also sources cache SRAM wafers from Cypress Semiconductor, and recently established a relationship with NEC for the production of wafers for the its ASIC products. In addition, ROSS has a procurement agreement with MicroModule Systems (MMS), which manufactures multi-die packages utilizing its advanced substrate technology. Multi-die packages are also manufactured for ROSS by nChip and Fujitsu. ROSS also routinely conducts discussions with additional manufacturers and suppliers to explore alternative sources for wafers, multi-die packages, CPU modules and motherboards. This manufacturing strategy provides it with access to state-of-the-art manufacturing processes and minimizes its capital expenditures, while enabling it to maintain the focus on its core competencies.

Identify and Pursue Non-Desktop Applications — In addition to workstations and servers, applications for hyperSPARC products include telecommunications, data communications, embedded systems and other non-desktop applications. ROSS customers in these non-desktop markets include Siemens (medical imaging equipment) and L.M. Ericsson (telephone messaging systems), among others. ROSS plans to continue to identify and pursue non-desktop applications as an added source of future growth for its hyperSPARC products.

Leverage Core Competencies into Other Desktop Markets — Its core competencies in RISC architecture, the design and integration of cache memory and control, multiprocessing technology, and advanced testing procedures provide ROSS with the ability to develop microprocessors and associated semiconductor products for other RISC and non-RISC desktop markets. For example, high-speed external cache memory, a core component of ROSS' SPARC products, is increasingly utilized in high-end PCs. ROSS has developed a 32-bit 150-MHz one megabyte cache SRAM, and has the capability to develop cache SRAMs for the PC market. ROSS may consider developing products for the PC and other desktop markets, as internal resources allow.

Products

The hyperSPARC family of microprocessors is ROSS Technology's principal product line. It sells hyperSPARC CPU products in two physical forms: as single and dual processor MBus module daughtercards (MBMs); and, to a lesser extent, as stand-alone multi-die packages for space and power-sensitive applications.

Multi-Die Packages — ROSS' hyperSPARC MDPs incorporate a complete CPU chipset: the RT620 Central Processing Unit; the RT625 or RT626 Cache Controller, Memory Management, and Tag Unit; and the RT627 or RT628 Cache Data Units. The hyperSPARC second-level caches are offered in 256 kilobyte, 512 kilobyte, and one megabyte direct-mapped configurations. The MDPs integrate six to 10 chips, including second level cache, into a single package. All hyperSPARC MDPs are fully multiprocessing capable. MDPs are purchased on a stand-alone basis for incorporation into space- and power-sensitive applications such as notebook computers, I/O subsystems, and embedded control.

MBus Modules — MDPs are typically sold to OEMs as part of an integrated solution: the MBus module (MBM). ROSS introduced the industry's first MBus module in 1990 to facilitate the open architectural, or "plug-and-play," advantages of the SPARC architecture. Its MBMs contain one or two hyperSPARC MDPs on a 3.30-inch X 5.78-inch CPU daughtercard that plugs into one of the MBus "sockets" of the system motherboard via a SPARC-standard MBus connector.

ROSS sells its MBMs into both the OEM and upgrade markets. The MBM approach allows OEM customers to be flexible in the machine configurations they offer to their end-user customers. The same motherboard design, which typically contains two MBus sockets, can accommodate one, two or four processors at any available speed for the targeted price/performance point. The marketplace success of MBus-based machines also provides the basis for the company's upgrade business, in which end users of Sun's SPARCstation 10 and 20 workstations and SPARCserver 600 class servers can realize the maximum value of their system investment by replacing the MBMs in their existing machines with the Company's higher-performance hyperSPARC MBMs.

ROSS' hyperSPARC products feature high-performance integer, floating-point and memory-management capabilities for multi-tasking operating environments. The hyperSPARC architecture is especially well-suited for applications that are floating-point-intensive, such as many scientific, computer-aided design, and seismic modeling applications. All hyperSPARC products conform to SPARC Version 8 Architecture (SPARC International's current commercially-adopted standard) specifications and offer full functionality — including multiprocessing — with both the SunOS (version 1.4.x) and Solaris (version 2.1.x) operating systems. Complete backwards software compatibility is an essential component of ROSS' marketing strategy.

Customers and Applications

ROSS sells its hyperSPARC products into two principal markets: the OEM market and the upgrade (end user) market.

OEM Market — OEM customers include a growing number of companies in several market segments that use ROSS' SPARC products in a variety of end products. The largest of these OEM market segments, computer workstations, historically has accounted for most of the company's OEM revenue (approximately 80 percent in fiscal 1995). Other OEM market segments addressed include high-performance network file servers, massively parallel systems, fault-tolerant systems, telecommunications, data communications and embedded systems.

The following table lists representative OEM customers that have purchased the Company's products to date, categorized by market segment and application. Many of these customers have purchased several products from the Company's product line.

<u>Market Segment</u>	<u>OEM</u>	<u>Application</u>
Workstations	Sun Microsystems, Fujitsu, Axil, ICL	Computer-Aided Design, Engineering, Client-Server Computing
Network File Servers	Auspex, Fujitsu, ICL	I/O File Server Hierarchical Storage
Massively Parallel Systems	Meiko Scientific Cray Research, Thinking Machines, ICL	Numerical Analysis, Large Database
Fault Tolerant Systems	Toshiba, Fujitsu	Banking, Switching
Data Communications	Ericsson Messaging Digital Switch (DSC) Fujitsu, GNP Computing	Phone Messaging Systems, Phone Databases
Embedded Systems	Siemens Medical, Tritec, Integrix, Force, Themis	MRI Processing, Process Control, Video Conferencing, Military

Upgrade Market — ROSS Technology's upgrade customer base is composed of the end users of SPARCstation 10 and 20 class workstations and SPARCserver 600 class workstation servers who wish to upgrade the performance of their existing machines. This customer base spans a wide range of applications and industries that reflect the variety of SPARC workstation and server users. By replacing the CPU daughtercard of their machines with one or two hyperSPARC upgrade modules, these users can experience a significant increase in the performance of their workstations. New hyperSTATION motherboard upgrades are now also available to owners of SPARCstation 5 machines. These upgrades incorporate two MBus slots that allow owners of these systems to enjoy the benefits of full multiprocessing (up to four CPUs) while keeping software investments intact.

The following table lists representative customers of ROSS upgrade products, categorized by industry.

<u>Industry</u>	<u>Upgrade Customer</u>
Financial Services	American Express Salomon Brothers
Oil and Gas	Amoco Chevron
Telecommunications	DSC Communications
Electronics	Advanced Micro Devices LSI Logic Motorola

Technology

Chipset Design — The company's design approach is first to apply advanced RISC architectural principles and implementation techniques, such as super-pipelining (the ability to execute both data transfer operations and instruction operations in a single clock cycle) and superscalar (the ability to launch multiple instructions in a single clock cycle), in defining the features and functions of its SPARC microprocessors, and then to partition the CPU's functionality into multiple die which are connected through the use of advanced multi-die packaging. As a result, ROSS chipsets contain a greater number of transistors, and correspondingly a greater level of performance and functionality, than are practical for single monolithic die. The company also designs its microprocessors to facilitate parallel processing at both the microarchitectural level (e.g., superscalar) and process level (e.g., multiprocessing). All hyperSPARC CPUs have full hardware support for multiprocessing. The hyperSPARC architecture uses simpler pipelines than those typically used by other microprocessor manufacturers, and ROSS' pipelines are consequently capable of running at higher clock speeds. This approach, as well as utilization of pure CMOS manufacturing processes, enable the hyperSPARC design to scale very effectively in clock frequency.

The cache architecture of hyperSPARC utilizes a primary cache on the company's microprocessor logic chip, and a secondary cache ranging from 256 kilobytes to one megabyte contained within the multi-die package. The secondary cache is composed of custom SRAM die specially designed to operate with the hyperSPARC microprocessor and cache controller chips. These SRAMs, as part of the CPU chipset, operate at the full clock frequency of the CPU and together with the hyperSPARC microprocessor transfer information in fewer clock cycles than is typically required by competing CPUs.

Multi-Die Packaging Technology — With each new product generation, semiconductor manufacturers are under pressure to produce microprocessors with higher performance and greater functionality, while maintaining or lowering their cost structure. ROSS has met these conflicting goals by utilizing multi-die packaging, which it developed cooperatively with key partners.

Multi-die packaging technology integrates multiple bare semiconductor die into a single integrated circuit package. Instead of driving high-frequency signals from

chip to chip across a printed circuit board (PCB), signals in a multi-die package travel millimeters through an advanced silicon or copper/polyimide substrate with only a fraction of the capacitive and inductive loads. This results in higher attainable clock speeds, a considerable reduction in power consumption, less capacitive loading and smaller board surface requirements. In addition, the reliability and speed of a chipset assembled in a MDP is greater than if implemented as separately-packaged chips. By successfully addressing fundamental limitations of conventional packaging, multi-die packaging simplifies systems and semiconductor designers' jobs. It also makes higher performance products possible without any modifications to existing die. MDPs are also more economical to manufacture because they utilize smaller die and improve effective yields by allowing die to be optimally matched (or "kitted") with other die.

ROSS custom designs each of the die contained in its hyperSPARC products for use in multi-die packages. This approach enables hyperSPARC products to obtain the maximum benefits of this advanced multi-die packaging technology.

Pure CMOS Implementation — ROSS executes each component of its hyperSPARC chipset — including its cache SRAMs — using pure CMOS. Although many of its competitors manufacture their CPU logic designs in pure CMOS, most incorporate bipolar transistors into their "CMOS" cache SRAMs (an approach called "BiCMOS"). Its pure CMOS approach, made possible by the use of multi-die packaging methodologies, enables the company's cache SRAMs and CPU chipsets to achieve greater clock speeds and performance at lower costs than are possible for SRAMs and chipsets incorporating BiCMOS.

The pure CMOS approach possesses several inherent advantages over BiCMOS:

Smaller Die Sizes and Lower Costs — Because of the greater masking, etching and implantation steps required to integrate bipolar transistors into a CMOS process, BiCMOS defect densities (as measured by defects per unit area of silicon) typically are higher (as much as 25 percent) than those for CMOS at a given level of processing capability. CMOS processes can also achieve significantly finer circuit geometries than BiCMOS processes, enabling CMOS circuits to run at higher speeds. The larger BiCMOS geometries also result in die sizes that are typically 20 percent to 40 percent larger than those of competing pure CMOS products. The larger BiCMOS die sizes, combined with higher BiCMOS defect densities, translate into a significant decrease in wafer yields and a significant increase in die unit costs.

Temperature and Performance — Due to the underlying physics of bipolar semiconductor junctions, as a BiCMOS device heats up it draws more current, which in turn escalates circuit temperature. BiCMOS devices therefore require special thermal sensing and protection circuits, which compromise clock speeds, but without which the "thermal runaway" phenomenon could eventually destroy a BiCMOS device. Pure CMOS devices, on the other hand, run faster and draw more current as environmental temperature decreases. As a result, pure CMOS devices run at lower temperatures than BiCMOS devices and do not require artificial slow-down circuitry to prevent them from self-destructing.

Cache Efficiency — In systems incorporating a traditional PCB interconnect between the microprocessor and cache memory, BiCMOS SRAMs are better able than pure CMOS SRAMs to drive the high capacitive loads of such systems, and therefore possess certain advantages despite their inherent cost and performance problems. The multi-die packaging design and manufacturing approach, which has eliminated the PCB interconnect, has enabled ROSS to reap the full benefits of its core competency in SRAM design and the inherent advantages of pure CMOS. As a result, the ROSS 256 kilobyte cache subsystem generally outperforms 512 kilobyte caches of other CPU manufacturers. Likewise, its 512 kilobyte cache generally outperforms the one megabyte caches of other CPU manufacturers. Finally, ROSS' one megabyte cache generally delivers better cache performance than other products currently on the market.

Decoupled MBus — In the early 1990s, traditional design cycles for system boards and support ASICs began to impede the ability of systems companies to deliver the full benefits of hyperbolically-increasing microprocessor performance. The first generation MBus-based microprocessor/cache subsystems (of which ROSS' 6002 product was the first) that existed at that time ran their CPU/cache clocks at the same speed as the system's master MBus clock. In order to increase the clock rate of the CPU/cache subsystem, the entire system had to be capable of a one-for-one increase in clock speed. In 1992, ROSS eliminated this performance roadblock by developing an asynchronous interface at the point of interface between the CPU/cache and the system MBus (the "decoupled MBus"). This development has enabled the company to supply to its OEM customers successive generations of microprocessor products running at progressively faster clock speeds from 55 to 150 Mhz over the past two years, without requiring any changes to the underlying system board design. The subsequent ability of its OEM customers to offer ever-increasing performance while maintaining their existing motherboard, chipset, and system box design and manufacturing investments is a considerable engineering and marketing advantage for ROSS. A similar protection of end-user investments has been achieved through MBus module replacement field upgrades of the existing installed base of workstations and servers.

Sales, Marketing and Support

Sales and Marketing — ROSS employs various channels of sales and distribution for its hyperSPARC product family. OEM sales are conducted through a direct sales force and a worldwide network of manufacturer representatives. Sales of upgrade products are conducted through both direct sales and manufacturer representative forces, as well as a worldwide network of value-added resellers.

The company's strategy for upgrade sales has been to focus its resources on the education and motivation of VARs, a cost-effective alternative to adding a large internal direct sales force. Major upgrade accounts have direct ROSS sales representation.

ROSS offers a warranty on its products in line with standard industry practice. Under the terms of this warranty, the company replaces or refunds the purchase price of any unit that fails to operate to published specifications, provided the unit is used within specified environmental operating parameters. The duration of this warranty is one year for OEM customers, and two years for upgrade customers.

Service and Technical Support — ROSS has two distinct channels of technical support to service the OEM and upgrade customer bases. Technical support for OEMs is provided through the company's Applications Engineering Department, which provides in-depth technical expertise to assist in the design, debugging, and performance analysis of systems under development by OEM customers. The upgrade technical support department includes a 1-800-ROSS-YES line directly into the company's support personnel, providing telephone support from 7:30 a.m. to 7:30 p.m. Central Time. This group provides pre- and post-sales assistance to upgrade prospects and customers. ROSS has engaged key service providers, including Digital Equipment and Computervision, to provide hardware support for ROSS products. In addition, the company has established partnerships with key software technology partners, such as SunSoft and Apogee, for technical support and system performance tuning.

Relationship with Fujitsu

Fujitsu has been the majority shareholder of ROSS Technology since July 1993, when it purchased the company from Cypress Semiconductor and other stockholders. At present, five out of nine of the ROSS board of directors are also employees of Fujitsu. The parent corporation is the second-largest computer manufacturer in the world, with approximately \$35 billion in annual revenues.

Management

Roger D. Ross, President, Chairman, Director — one of the founders of the company, he has been the president, chairman of the board and a director since the company's inception in 1988. Prior to founding the company, Mr. Ross spent five years at Motorola, Inc., serving as general manager for the Advanced Microprocessor Operation. He was also responsible for the Motorola 88000 RISC microprocessor program. Earlier, Mr. Ross spent nine years at NCR Corporation, where he served in various positions, including as engineering director for the NCR 7000 Fault Tolerant Computer System. He holds a bachelor of science degree in abstract mathematics, cum laude, from Ohio University, and has greater than 20 years of experience in the computer and microprocessor industries.

Mitchell K. Alsup, Chief Architect — Since joining the company in 1991, Mr. Alsup has been responsible for architectural development of the hyperSPARC line of microprocessors, has acted as chief scientist, has advanced circuit design techniques, and has performed technical marketing duties. Prior to joining ROSS Technology, Mr. Alsup spent 10 years at Motorola, Inc., where, among other duties, he was the principal designer of Motorola's 88000 line of microprocessors. Mr. Alsup also spent three years at NCR as a project leader. He received a bachelor of science in electrical engineering degree in 1975 from Carnegie-Mellon University.

Trevor S. Smith, Vice President of Product Development — One of the founders of ROSS Technology, Mr. Smith has acted as vice president of silicon design since the company's inception. Earlier, he spent three years with Motorola, Inc., serving as, among other things, manager of MPU standard cell cores and cell library development, and three years at ICL, one of Europe's largest computer systems suppliers, where he served as manager of CPU development for Emitter Coupled Logic (a high speed bipolar transistor-based technology) and CMOS mainframe

CPUs. He received a bachelor of science degree in physics and electronic engineering from the University of Manchester, England, and has greater than 18 years of experience in the computer and microprocessor industries.

Joe D. Jones, Vice President of Operations — Mr. Jones joined the Company in 1991 as the director of quality assurance, and in 1993 assumed his current position. Earlier, he served for five years with Cypress Semiconductor Corporation, a producer of semiconductor electronic devices, as quality assurance manager, in addition to four years with Advanced Micro Devices in various engineering and management positions. Mr. Jones received a bachelor of science degree in chemical engineering from the University of Texas at Austin and has approximately 13 years of experience in the computer and microprocessor industries.

Matthew R. Gutierrez, Vice President of Marketing— Mr. Gutierrez joined the Company in 1989 as an applications engineer and has since held various other positions with the Company including Applications Engineering Manager, Manager of Product Marketing, Director of Product Marketing, and now Vice President of Marketing. Prior to joining the Company, Mr. Gutierrez served five years with General Motors Corporation where he held various engineering and test positions. Mr. Gutierrez holds a B.S. in Electrical Engineering from GMI Engineering and Management Institute and a M.S. in Electrical Engineering from the University of Texas at Austin.

ROSS History

ROSS Technology is a majority-owned subsidiary of Fujitsu, Ltd., its largest shareholder. A minority position in ROSS Technology is also held by Sun Microsystems. Functioning autonomously, ROSS is fully responsible for all operational aspects of its SPARC programs. The company's objective is to drive SPARC, the industry's highest volume reduced instruction set computing (RISC) architecture, to increased performance leadership and marketshare in the late 1990's. ROSS is one of the industry's most prominent suppliers of SPARC™ microprocessors and microprocessor-related products to both OEM and end-user markets.