



# Sil3512 PCI to Serial ATA Controller Data Sheet

June 2006

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### Revision History

Revision	Date	Comment
A	01/26/04	Derived from Preliminary datasheet Rev 0.98
B	06/20/06	Removed Sil3512CT128 (128 pin TQFP standard package without an exposed pad) Corrected inconsistent sentences (minor fixes including mistyping)
C	06/28/06	Updated Template, removed confidential markings

# Table of Contents

<b>1</b>	<b>Overview</b>	<b>6</b>
1.1	Key Benefits	6
1.2	Features	6
1.2.1	Overall Features	6
1.2.2	PCI Features	6
1.2.3	Serial ATA Features	6
1.2.4	Other Features	7
1.3	Applications	7
1.4	References	7
1.5	Functional Description	7
1.6	Functional Block Diagram	7
1.7	PCI Interface	8
1.8	PCI Initialization	8
1.9	PCI Bus Operations	8
1.10	PCI Configuration Space	9
1.11	Deviations from the Specification	9
<b>2</b>	<b>Electrical Characteristics</b>	<b>10</b>
2.1	Device Electrical Characteristics	10
2.2	SATA Interface Timing Specifications	11
2.3	SATA Interface Transmitter Output Jitter Characteristics	12
2.4	CLKI SerDes Reference Clock Input Requirements	12
2.5	PCI 33 MHz Timing Specifications	13
2.6	PCI 66 MHz Timing Specifications	13
2.7	Flash Memory Timing Specifications	14
<b>3</b>	<b>Pin Definition</b>	<b>15</b>
3.1	Sil3512 Pin Listing	15
3.2	Sil3512 Pin Diagram	19
3.3	Sil3512 Pin Descriptions	20
3.3.1	PCI 66MHz 32-bit	20
3.3.2	Miscellaneous I/O	22
3.3.3	Serial ATA Signals	23
<b>4</b>	<b>Package Drawing</b>	<b>25</b>
<b>5</b>	<b>Enhanced Packaging (only for Sil3512ECTU128)</b>	<b>26</b>
5.1	PCB Design Requirements	26
<b>6</b>	<b>Block Diagram</b>	<b>29</b>
<b>7</b>	<b>Auto-Initialization</b>	<b>30</b>
7.1	Auto-Initialization from FLASH	30
7.2	Auto-Initialization from EEPROM	31
<b>8</b>	<b>ATA Command Supported</b>	<b>33</b>
8.1	Data Modes	33
8.2	ATA Commands	33

## Table of Tables

Table 2-1 Absolute Maximum Ratings.....	10
Table 2-2 DC Specifications.....	10
Table 2-3 SATA Interface DC Specifications.....	11
Table 2-4 SATA Interface Timing Specifications.....	11
Table 2-6 SATA Interface Transmitter Output Jitter Characteristics – Sil3512ECTU128 (EPAD is soldered to a landing area on the PCB).....	12
Table 2-7 CLKI SerDes Reference Clock Input Requirements.....	12
Table 2-8 PCI 33 MHz Timing Specifications.....	13
Table 3-1 Sil3512 Pin Listing.....	18
Table 3-3 Pin Types.....	18
Table 7-1 Auto-Initialization from Flash Timing.....	30
Table 7-2 Flash Data Description.....	31
Table 7-3 Auto-Initialization from EEPROM Timing.....	32
Table 7-4 Auto-Initialization from EEPROM Timing Symbols.....	32
Table 7-5 EEPROM Data Description.....	32
Table 8-1 Supported ATA Commands.....	33

## Table of Figures

Figure 1-1 : Sil3512 Block Diagram.....	7
Figure 1-2: Address Lines During Configuration Cycle.....	9
Figure 2-1 Flash Memory Timing.....	14
Figure 3-1. Sil3512 Pin Diagram .....	19
Figure 4-1: Package Drawing – 128 TQFP.....	25
Figure 5-1: Top View of Enhanced 128-pin TQFP Package.....	26
Figure 5-2: Top View of TQFP Landing area Design on PCB .....	27
Figure 5-3: Ground Pad Via Grid.....	27
Figure 5-4: Top View of Recommended Stencil Design .....	28
Figure 6-1: Sil3512 Block Diagram.....	29
Figure 7-1 Auto-Initialization from Flash Timing .....	30
Figure 7-2 Auto-Initialization from EEPROM Timing .....	31

# 1 Overview

The Silicon Image Sil3512 is a single-chip solution for a PCI to Serial ATA controller. It accepts host commands through the PCI bus, processes them and transfers data between the host and Serial ATA devices. It can be used to control two independent Serial ATA channels. Each channel has its own Serial ATA bus and will support one Serial ATA device. The Sil3512 supports a 32-bit 66 MHz PCI bus and the Serial ATA Generation 1 transfer rate of 1.5 Gb/s (150 MB/s).

## 1.1 Key Benefits

The Silicon Image Sil3512 PCI to Serial ATA Controller is the perfect single-chip solution for designs that need to accommodate storage peripherals with the new Serial ATA interface. Any system with a PCI bus interface can simply add the Serial ATA interface by adding a card with the Sil3512 and loading the driver into the system.

The Sil3512 comes complete with drivers for Windows 98, Windows Millennium, Windows NT 4.0, Windows 2000, XP, Windows 2003, Netware 5.1, 6.0, 6.5, Red Hat Linux 8.0, 9.0, SuSE Linux 8.1, 8.2 and United Linux 1.0.

## 1.2 Features

### 1.2.1 Overall Features

- Standalone PCI to Serial ATA host controller chip
- Compliant with PCI Specification, revision 2.3.
- Compliant with Programming Interface for Bus Master IDE Controller, revision 1.0.
- Driver support for Windows 98, Windows Millennium, Windows NT 4.0, Windows 2000, XP, Windows 2003, Netware 5.1, 6.0, 6.5, Red Hat Linux 8.0, 9.0, SuSE Linux 8.1, 8.2 and United Linux 1.0
- Supports up to 4Mbit external FLASH or EPROM for BIOS expansion.
- Supports an external EEPROM, FLASH or EPROM for programmable device ID, subsystem vendor ID, subsystem product ID and PCI sub-class code.
- Supports the Silicon Image specific driver for special chip functions.
- Fabricated in a 0.18 $\mu$ m CMOS process with a 1.8 volt core and 3.3 volt (5V tolerant) I/Os.
- Supports Plug and Play.
- Supports ATAPI device
- Supports Activity LEDs, one for each channel with 12mA open drain driving capability.
- Sil3512ECTU128 is available in a 128-pin TQFP package with e-pad. **EPAD must be soldered to PCB GND.**

### 1.2.2 PCI Features

- Supports 66 MHz PCI with 32-bit data.
- Supports PCI PERR and SERR reporting.
- Supports PCI bus master operations: Memory Read, Memory Read Multiple, and Memory Write.
- Supports PCI bus target operations: Configuration Read, Configuration Write, I/O Read, I/O Write, Memory Read, Memory Write, Memory Read Line (Memory Read) and Memory Read Multiple (Memory Read)
- Supports byte alignment for odd-byte PCI address access.
- Supports jumper configurable PCI class code.
- Supports programmable and EEPROM, FLASH and EPROM loadable PCI class code.
- Supports Base Address Register 5 in memory space.

### 1.2.3 Serial ATA Features

- Integrated Serial ATA Link and PHY logic
- Compliant with Serial ATA 1.0 specifications
- Supports two independent Serial ATA channels.
- Supports Serial ATA Generation 1 transfer rate of 1.5Gb/s.
- Supports Spread Spectrum in receiver
- Single PLL architecture, 1 PLL for both ports
- Programmable drive strengths for Backplane applications

### 1.2.4 Other Features

- Features independent 256-byte FIFOs (32-bit x 64 deep) per Serial ATA channel for host reads and writes.
- Features Serial ATA to PCI interrupt masking.
- Features Watch Dog Timer for fault resiliency.

## 1.3 Applications

- PC motherboards
- Serial ATA drive add on cards
- Serial ATA RAID controllers

## 1.4 References

For more details about the Serial ATA technology, the reader is referred to the following industry specifications:

- Serial ATA / High Speed Serialized AT Attachment specification, Revision 1.0
- PCI Local Bus Specification Revision 2.3
- Advanced Power Management Specification Revision 1.0
- PCI IDE Controller Specification Revision 1.0
- Programming Interface for Bus Master IDE Controller, Revision 1.0

## 1.5 Functional Description

Sil3512 is a PCI-to-Serial ATA controller chip that transfers data between the PCI bus and storage media (e.g. hard disk drive, etc). The Sil3512 consists of the following functional blocks:

- PCI Interface. Provides the interface to any system that has a PCI bus. Instructions and system clocks are based on this interface.
- Serial ATA Interface. Two separate channels (Primary and Secondary) to access storage media such as hard disk drive, floppy disk drive, CD-ROM.

## 1.6 Functional Block Diagram

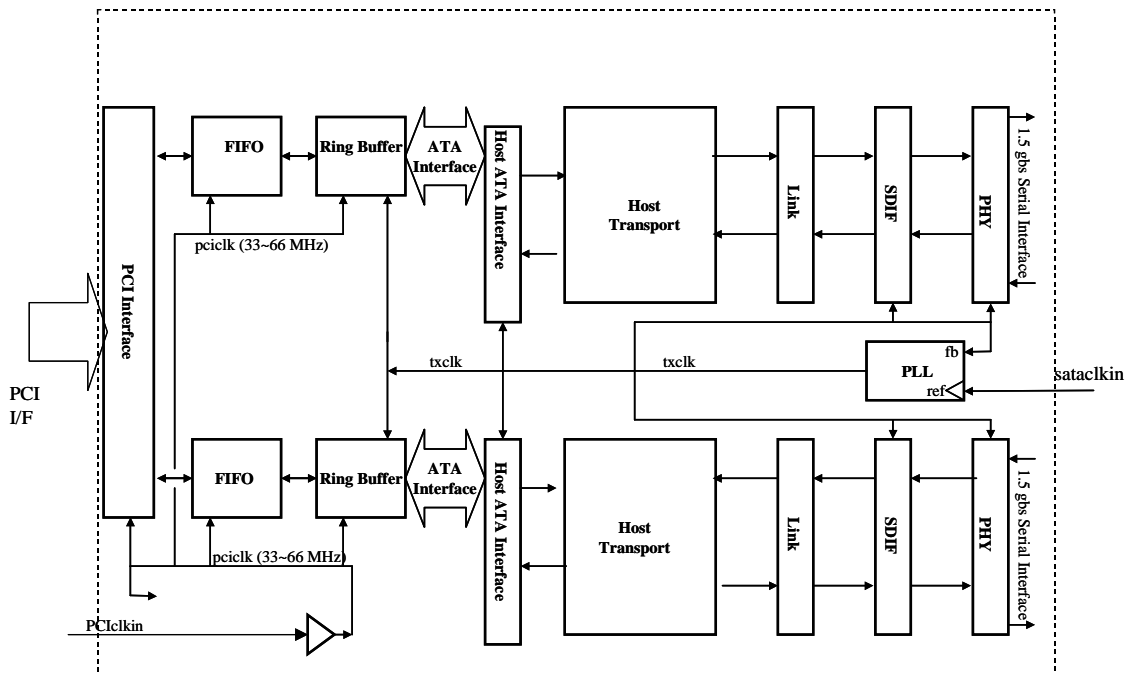


Figure 1-1 : Sil3512 Block Diagram

## 1.7 PCI Interface

The Sil3512 PCI interface is compliant with the PCI Local Bus Specification (Revision 2.3). The Sil3512 can act as a PCI master and a PCI slave, and contains the Sil3512 PCI configuration space and internal registers. When the Sil3512 needs to access shared memory, it becomes the bus master of the PCI bus and completes the memory cycle without external intervention. In the mode when it acts as a bridge between the PCI bus and the Serial ATA bus it will behave as a PCI slave.

## 1.8 PCI Initialization

Generally, when a system initializes a module containing a PCI device, the configuration manager reads the configuration space of each PCI device on the PCI bus. Hardware signals select a specific PCI device based on a bus number, a slot number, and a function number. If a device that is addressed (via signal lines) responds to the configuration cycle by claiming the bus, then that function's configuration space is read out from the device during the cycle. Since any PCI device can be a multifunction device, every supported function's configuration space needs to be read from the device. Based on the information read, the configuration manager will assign system resources to each supported function within the device. Sometimes new information needs to be written into the function's configuration space. This is accomplished with a configuration write cycle.

## 1.9 PCI Bus Operations

Sil3512 behaves either as a PCI master or a PCI slave device at any time and switches between these modes as required during device operation.

As a PCI slave, the Sil3512 responds to the following PCI bus operations:

- I/O Read
- I/O Write
- Configuration Read
- Configuration Write
- Memory Read
- Memory Write

All other PCI cycles are ignored by the Sil3512.

As a PCI master, the Sil3512 generates the following PCI bus operations:

- Memory Read Multiple
- Memory Read
- Memory Write



## 1.10 PCI Configuration Space

This section describes how the Sil3512 implements the required PCI configuration register space. The intent of PCI configuration space definition is to provide an appropriate set of configuration registers that satisfy the needs of current and anticipated system configuration mechanisms, without specifying those mechanisms or otherwise placing constraints on their use. These registers allow for:

- Full device relocation (including interrupt binding)
- Installation, configurations, and booting without user interventions
- System address map construction by device-independent software

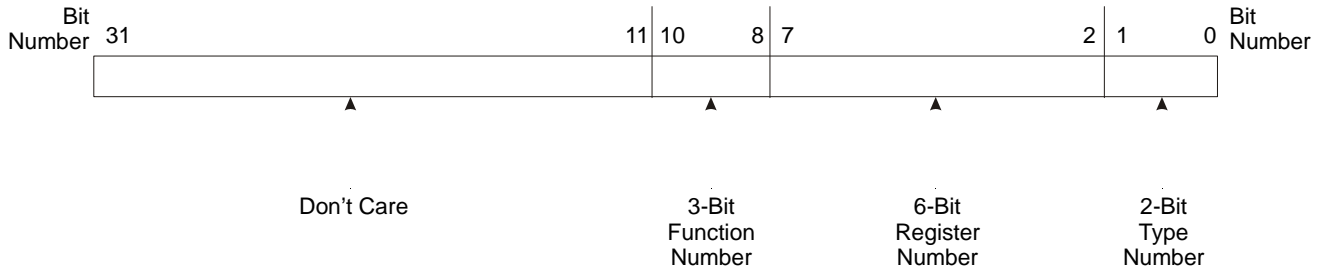


Figure 1-2: Address Lines During Configuration Cycle

Sil3512 only responds to Type 0 configuration cycles. Type 1 cycles, which pass a configuration request on to another PCI bus, are ignored.

The address phase during a Sil3512 configuration cycle indicates the function number and register number being addressed which can be decoded by observing the status of the address lines AD[31:0].

The value of the signal lines AD[7:2] during the address phase of configuration cycles selects the register of the configuration space to access. Valid values are between 0 and 15, inclusive. Accessing registers outside this range results in an all-0s value being returned on reads, and no action being taken on writes.

The Class Code register contains the Class Code, Sub-Class Code, and Register-Level Programming Interface registers.

All writable bits in the configuration space are reset to 0 by the hardware reset, PCI RESET (RST#) asserted. After reset, Sil3512 is disabled and will only respond to PCI configuration write and PCI configuration read cycles.

## 1.11 Deviations from the Specification

The Sil3512 product has been developed and tested to the specification listed in this document. As a result of testing and customer feedback, we may become aware of deviations to the specification that could affect the component's operation. To ensure awareness of these deviations by anyone considering the use of the Sil3512, we have included an Errata section at the end of this specification. Please ensure that the Errata section is carefully reviewed. It is also important that you have the most current version of this specification. If there are any questions, please contact Silicon Image, Inc.

## 2 Electrical Characteristics

### 2.1 Device Electrical Characteristics

Specifications are for Commercial Temperature range, 0°C to +70°C, unless otherwise specified.

Symbol	Parameter	Ratings	Unit
VDDO, VDDX	I/O and Oscillator Supply Voltage	4.0	V
VDDI, VDDA, VDDP	Digital, Analog and PLL Supply Power	2.15	V
V <sub>PCI_IN</sub>	Input Voltage for PCI signals	-0.3 ~ 6.0	V
V <sub>NONPCI_IN</sub>	Input Voltage for Non-PCI signals	-0.3 ~ VDDO+0.3	V
V <sub>CLK_IN</sub>	Input Voltage for CLKI	-0.3 ~ VDDX+0.3	V
I <sub>OUT</sub>	DC Output Current	16	mA
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	46.3	°C/W
T <sub>STG</sub>	Storage Temperature	-65 ~ 150	°C

Table 2-1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Type	Limits			Unit
				Min	Typ	Max	
VDDI, VDDA, VDDP	Supply Voltage (Digital, Analog, PLL)			1.71	1.8	1.89	V
VDDO	Supply Voltage(I/O)	-	-	3.0	3.3	3.6	V
IDD <sub>1.8V</sub>	1.8V Supply Current				236 <sup>1</sup>	330 <sup>2</sup>	mA
IDD <sub>3.3V</sub>	3.3V Supply Current	C <sub>LOAD</sub> = 20pF			12 <sup>1</sup>	30 <sup>2</sup>	mA
V <sub>IH</sub>	Input High Voltage	-	3.3V PCI	0.5xVDDO	-	-	V
		-	Non-PCI	2.0	-	-	
V <sub>IL</sub>	Input Low Voltage	-	3.3V PCI	-	-	0.3xVDDO	V
		-	Non-PCI	-	-	0.8	
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = -500uA	3.3V PCI	0.9xVDDO	-	-	V
		-	Non-PCI	2.4	-	-	
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> = 1500uA	3.3V PCI	-	-	0.1xVDDO	V
		-	Non-PCI	-	-	0.4	
V <sub>+</sub>	Input High Voltage	-	Schmitt	-	1.8	2.3	V
V <sub>-</sub>	Input Low Voltage	-	Schmitt	0.5	0.9	-	V
V <sub>H</sub>	Hysteresis Voltage	-	Schmitt	0.4	-	-	V
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = VDD	-	-10	-	10	uA
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = VSS	-	-10	-	10	uA
I <sub>ILOD</sub>	Open Drain output sync current					12	mA
I <sub>OZ</sub>	3-State Leakage Current	-	-	-10	-	10	uA

Notes:<sup>1</sup> Using the random data pattern (read/write operation) at 1.8V or 3.3V power supply, PCI interface = 33MHz

<sup>2</sup> Using the maximum toggling data pattern (read/write operation) at 1.89V or 3.6V power supply, PCI interface = 66MHz

Table 2-2 DC Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V <sub>DOUT_00</sub>	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 00	400	500	600	mV
V <sub>DOUT_01</sub>	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 01	500	600	700	mV
V <sub>DOUT_10</sub>	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 10	550	700	800	mV
V <sub>DOUT_11</sub>	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 11	650	800	900	mV
V <sub>DIN</sub>	RX+/RX- differential peak-to-peak input sensitivity		325			mV
V <sub>DIH</sub>	RX+/RX- differential Input common-mode voltage		200	300	450	mV
V <sub>DOH</sub>	TX+/TX- differential Output common-mode voltage		200	300	450	mV
V <sub>SdT</sub>	Squelch detector threshold		100	50	200	mV
Z <sub>DIN</sub>	Differential input impedance	REXT = 1k 1% for 25MHz SerDes Ref Clk REXT = 4.99k 1% for 100MHz SerDes Ref Clk	85	100	115	ohms
Z <sub>DOUT</sub>	Differential output impedance	REXT = 1k 1% for 25MHz SerDes Ref Clk REXT = 4.99k 1% for 100MHz SerDes Ref Clk	85	100	115	ohms

Table 2-3 SATA Interface DC Specifications

## 2.2 SATA Interface Timing Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
T <sub>TX_RISE_FALL</sub>	Rise and Fall time at transmitter	20%-80%	133		274	ps
T <sub>TX_SKEW</sub>	Tx differential skew				20	ps
T <sub>TX_DC_FREQ</sub>	Tx DC clock frequency skew		-350		+350	ppm
T <sub>TX_AC_FREQ</sub>	Tx AC clock frequency skew	SerDes Ref Clk = SSC AC modulation, subject to the "Downspread SSC" triangular modulation (30-33KHz) profile per 6.6.4.5 in SATA 1.0 specification	-5000		+0	ppm

Table 2-4 SATA Interface Timing Specifications

### 2.3 SATA Interface Transmitter Output Jitter Characteristics

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
RJ <sub>5UI</sub>	5UI later Random Jitter	Measured at Tx output pins 1sigma deviation		7.0		ps rms
RJ <sub>250UI</sub>	250UI later Random Jitter	Measured at Tx output pins 1sigma deviation		9.5		ps rms
DJ <sub>5UI</sub>	5UI later Deterministic Jitter	Measured at Tx output pins peak to peak phase variation Random data pattern		33		ps
DJ <sub>250UI</sub>	250UI later Deterministic Jitter	Measured at Tx output pins peak to peak phase variation Random data pattern		34		ps

Table 2-5 SATA Interface Transmitter Output Jitter Characteristics – Sil3512ECTU128 (EPAD is soldered to a landing area on the PCB)

### 2.4 CLKI SerDes Reference Clock Input Requirements

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
T <sub>CLKI_FREQ</sub>	Nominal Frequency	REXT = 1k 1% REXT = 4.99k 1%		25 100		MHz
T <sub>CLKI_J</sub>	CLKI frequency tolerance		-100		+100	ppm
T <sub>CLKI_RISE_FALL</sub>	Rise and Fall time at CLKI	25MHz reference clock, 20%-80% 100MHz reference clock, 20%-80%			4 2	ns
T <sub>CLKI_RC_DUTY</sub>	CLKI duty cycle	20%-80%	40		60	%

Table 2-6 CLKI SerDes Reference Clock Input Requirements

## 2.5 PCI 33 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T <sub>VAL</sub>	CLK to Signal Valid – Bussed Signals	2.0	11.0	ns
T <sub>VAL (PTP)</sub>	CLK to Signal Valid – Point to Point	2.0	11.0	ns
T <sub>ON</sub>	Float to Active Delay	2.0	-	ns
T <sub>OFF</sub>	Active to Float Delay	-	28.0	ns
T <sub>SU</sub>	Input Setup Time – Bussed Signals	7.0	-	ns
T <sub>SU (PTP)</sub>	Input Setup Time – Point to Point	10.0	-	ns
T <sub>H</sub>	Input Hold Time	0.0	-	ns

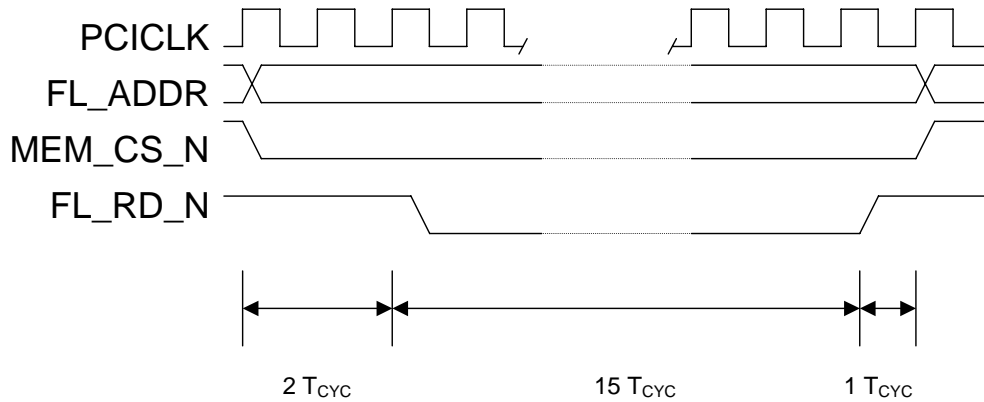
Table 2-7 PCI 33 MHz Timing Specifications

## 2.6 PCI 66 MHz Timing Specifications

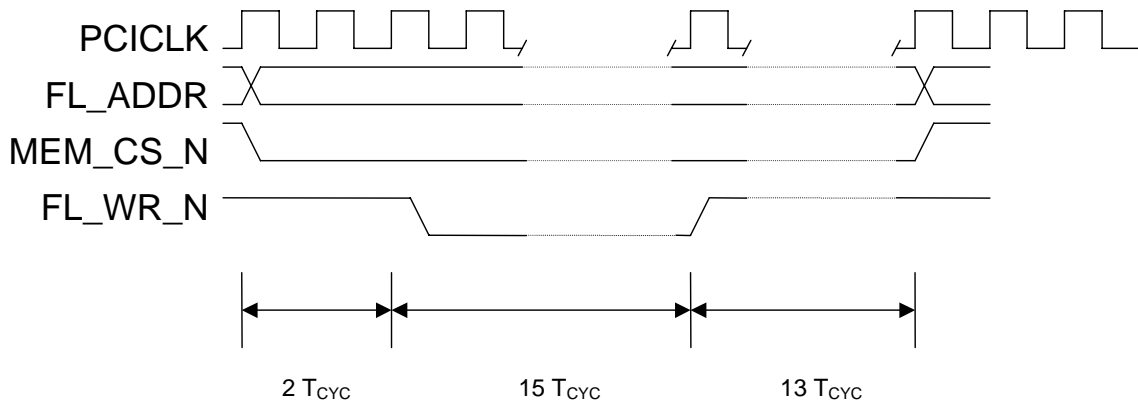
Symbol	Parameter	Limits		Unit
		Min	Max	
T <sub>VAL</sub>	CLK to Signal Valid – Bussed Signals	2.0	6.0	ns
T <sub>VAL (PTP)</sub>	CLK to Signal Valid – Point to Point	2.0	6.0	ns
T <sub>ON</sub>	Float to Active Delay	2.0		ns
T <sub>OFF</sub>	Active to Float Delay		14.0	ns
T <sub>SU</sub>	Input Setup Time – Bussed Signals	3.0		ns
T <sub>SU (PTP)</sub>	Input Setup Time – Point to Point	5.0		ns
T <sub>H</sub>	Input Hold Time	0.0		ns

Table 2-8 PCI 66 MHz Timing Specifications

## 2.7 Flash Memory Timing Specifications



### FLASH READ TIMING



### FLASH WRITE TIMING

Figure 2-1 Flash Memory Timing

## 3 Pin Definition

### 3.1 Sil3512 Pin Listing

This section describes the pin-out of the Sil3512 PCI-to-Serial ATA host controller. Table 3-1 Sil3512 Pin Listing gives the pin numbers, pin names, pin types, drive types where applicable, internal resistors where applicable, and descriptions.

Pin #	Pin Name	Type	Internal Resistor	Description
1	PCI_AD00	I/O	-	PCI Address/Data
2	EEPROM_SDAT	I/O	PU – 70k	EEPROM Serial Data
3	EEPROM_SCLK	I/O	PU – 70k	EEPROM Serial Clock
4	VDDA	PWR	-	1.8V SerDes Power
5	RxP2	I		Channel 2 Differential Receive +ve
6	RxN2	I		Channel 2 Differential Receive -ve
7	GND A	GND	-	Analog Ground
8	VDDA	PWR	-	1.8V SerDes Power
9	GND A	GND	-	Analog Ground
10	TxN2	O		Channel 2 Differential Transmit -ve
11	TxP2	O		Channel 2 Differential Transmit +ve
12	GND A	GND	-	Analog Ground
13	VDDA	PWR	-	1.8V SerDes Power
14	RxP1	I		Channel 1 Differential Receive +ve
15	RxN1	I		Channel 1 Differential Receive -ve
16	GND A	GND	-	Analog Ground
17	VDDA	PWR	-	1.8V SerDes Power
18	GND A	GND	-	Analog Ground
19	TxN1	O		Channel 1 Differential Transmit -ve
20	TxP1	O		Channel 1 Differential Transmit +ve
21	GND A	GND	-	Analog Ground
22	VDDP	PWR	-	1.8V PLL Power
23	VDDP	PWR	-	1.8V PLL Power
24	REXT	I		External Reference Resistor Input
25	GND A	GND	-	Analog Ground
26	XTALI/CLKI	I		Crystal Oscillator Input or external clock input
27	XTALO	O		Crystal Oscillator Output
28	VDDO	PWR		3.3V supply for Crystal Oscillator
29	SCAN_EN	I	PD – 60k	Internal Scan Enable
30	MEM_CS_N	O	PU – 70k	Memory Chip Select

Pin #	Pin Name	Type	Internal Resistor	Description
31	FL_ADDR[00] / IDE_CFG	I/O	PU – 70k	Flash Memory Address 0 / IDE-RAID Configuration
32	FL_ADDR[01] / BA5_EN	I/O	PU – 70k	Flash Memory Address 1 / Base Address Register 5 Enable
33	FL_ADDR[02]	O	PU – 70k	Flash Memory Address 2
34	FL_WR_N	O	PU – 70k	Flash Memory Write Strobe
35	FL_RD_N	O	PU – 70k	Flash Memory Read Strobe
36	FL_ADDR[03]	O	PU – 70k	Flash Memory Address 3
37	FL_ADDR[04]	O	PU – 70k	Flash Memory Address 4
38	FL_ADDR[05]	O	PU – 70k	Flash Memory Address 5
39	FL_ADDR[06]	O	PU – 70k	Flash Memory Address 6
40	VDDO	PWR	-	3.3 Volt Power
41	VSS	GND	-	Ground
42	FL_ADDR[07]	O	PU – 70k	Flash Memory Address 7
43	FL_ADDR[08]	O	PU – 70k	Flash Memory Address 8
44	FL_ADDR[09]	O	PU – 70k	Flash Memory Address 9
45	FL_ADDR[10]	O	PU – 70k	Flash Memory Address 10
46	FL_ADDR[11]	O	PU – 70k	Flash Memory Address 11
47	VDDI	PWR	-	1.8V Internal core Power
48	VSS	GND	-	Ground
49	FL_ADDR[12]	O	PU – 70k	Flash Memory Address 12
50	FL_ADDR[13]	O	PU – 70k	Flash Memory Address 13
51	LED0	OD		Channel 0 activity LED indicator
52	FL_ADDR[14]	O	PU – 70k	Flash Memory Address 14
53	FL_ADDR[15]	O	PD – 60k	Flash Memory Address 15
54	FL_ADDR[16]	O	PD – 60k	Flash Memory Address 16
55	FL_ADDR[17]	O	PD – 60k	Flash Memory Address 17
56	FL_ADDR[18]	O	PD – 60k	Flash Memory Address 18
57	TEST_MODE	I	PD – 60k	Test Mode Enable
58	FL_DATA[00]	I/O	PU – 70k	Flash Memory Data 0
59	FL_DATA[01]	I/O	PU – 70k	Flash Memory Data 1
60	FL_DATA[02]	I/O	PU – 70k	Flash Memory Data 2
61	FL_DATA[03]	I/O	PU – 70k	Flash Memory Data 3
62	FL_DATA[04]	I/O	PU – 70k	Flash Memory Data 4
63	FL_DATA[05]	I/O	PU – 70k	Flash Memory Data 5
64	FL_DATA[06]	I/O	PU – 70k	Flash Memory Data 6
65	FL_DATA[07]	I/O	PU – 70k	Flash Memory Data 7
66	LED1	OD		Channel 1 activity LED indicator
67	PCI_INTA_N	OD	-	PCI Interrupt



Pin #	Pin Name	Type	Internal Resistor	Description
68	PCI_RST_N	I-Schmitt	-	PCI Reset
69	PCI_CLK	I	-	PCI Clock
70	PCI_GNT_N	I	-	PCI Bus Grant
71	PCI_REQ_N	T	-	PCI Bus Request
72	PCI_AD31	I/O	-	PCI Address/Data
73	PCI_AD30	I/O	-	PCI Address/Data
74	PCI_AD29	I/O	-	PCI Address/Data
75	VDDO	PWR	-	3.3 Volt Power
76	VSS	GND	-	Ground
77	PCI_AD28	I/O	-	PCI Address/Data
78	PCI_AD27	I/O	-	PCI Address/Data
79	PCI_AD26	I/O	-	PCI Address/Data
80	VDDI	PWR	-	1.8V Internal Core Power
81	VSS	GND	-	Ground
82	PCI_AD25	I/O	-	PCI Address/Data
83	PCI_AD24	I/O	-	PCI Address/Data
84	PCI_CBE3	I/O	-	PCI Command/Byte Enable
85	PCI_IDSEL	I	PU-70K	PCI ID Select
86	PCI_AD23	I/O	-	PCI Address/Data
87	PCI_AD22	I/O	-	PCI Address/Data
88	PCI_AD21	I/O	-	PCI Address/Data
89	PCI_AD20	I/O	-	PCI Address/Data
90	PCI_AD19	I/O	-	PCI Address/Data
91	VDDO	PWR	-	3.3 Volt Power
92	VSS	GND	-	Ground
93	PCI_AD18	I/O	-	PCI Address/Data
94	PCI_AD17	I/O	-	PCI Address/Data
95	PCI_AD16	I/O	-	PCI Address/Data
96	PCI_CBE2	I/O	-	PCI Command/Byte Enable
97	PCI_FRAME_N	I/O	-	PCI Frame
98	PCI_IRDY_N	I/O	-	PCI Initiator Ready
99	PCI_PERR_N	I/O	-	PCI Parity Error
100	PCI_STOP_N	I/O	-	PCI Stop
101	PCI_DEVSEL_N	I/O	-	PCI Device Select
102	PCI_TRDY_N	I/O	-	PCI Target Ready
103	PCI_SERR_N	OD	-	PCI System Error
104	PCI_PAR	I/O	-	PCI Parity
105	PCI_CBE1	I/O	-	PCI Command/Byte Enable
106	VDDO	PWR	-	3.3 Volt Power

Pin #	Pin Name	Type	Internal Resistor	Description
107	VSS	GND	-	Ground
108	PCI_AD15	I/O	-	PCI Address/Data
109	PCI_AD14	I/O	-	PCI Address/Data
110	PCI_AD13	I/O	-	PCI Address/Data
111	PCI_AD12	I/O	-	PCI Address/Data
112	VDDI	PWR	-	1.8 Volt Core Power
113	VSS	GND	-	Ground
114	PCI_AD11	I/O	-	PCI Address/Data
115	PCI_AD10	I/O	-	PCI Address/Data
116	PCI_M66EN	I	PU-70K	PCI 66 MHz Enable
117	PCI_AD09	I/O	-	PCI Address/Data
118	PCI_AD08	I/O	-	PCI Address/Data
119	PCI_CBE0	I/O	-	PCI Command/Byte Enable
120	PCI_AD07	I/O	-	PCI Address/Data
121	PCI_AD06	I/O	-	PCI Address/Data
122	VDDO	PWR	-	3.3 Volt Power
123	VSS	GND	-	Ground
124	PCI_AD05	I/O	-	PCI Address/Data
125	PCI_AD04	I/O	-	PCI Address/Data
126	PCI_AD03	I/O	-	PCI Address/Data
127	PCI_AD02	I/O	-	PCI Address/Data
128	PCI_AD01	I/O	-	PCI Address/Data

**Table 3-1 Sil3512 Pin Listing**

Pin Type	Pin Description
I	Input Pin with LVTTTL Thresholds
I-Schmitt	Input Pin with Schmitt Trigger
O	Output Pin
T	Tri-state Output Pin
I/O	Bi-directional Pin
OD	Open Drain Output Pin

**Table 3-2 Pin Types**

PCI pins are 5V tolerant.

### 3.2 Sil3512 Pin Diagram

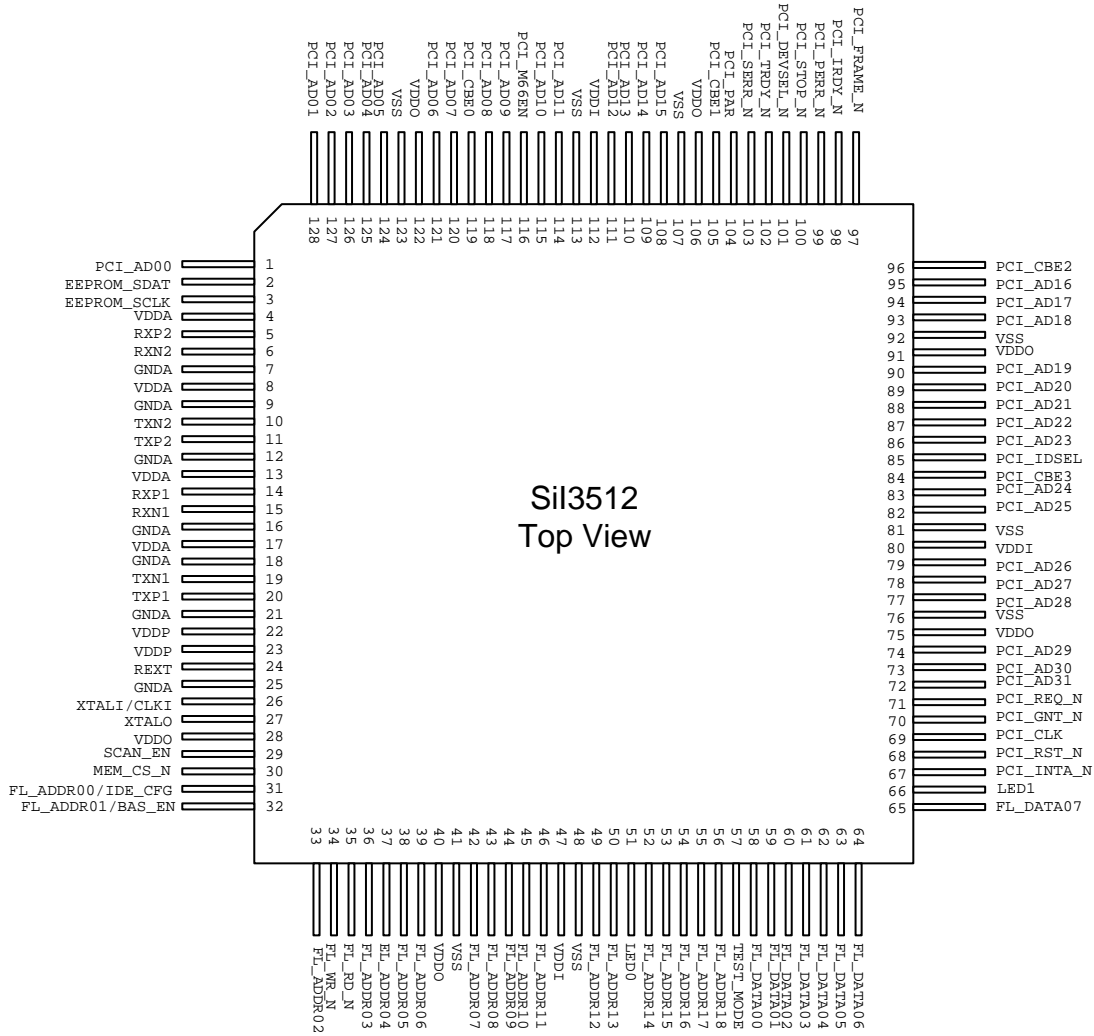


Figure 3-1. Sil3512 Pin Diagram

## 3.3 Sil3512 Pin Descriptions

### 3.3.1 PCI 66MHz 32-bit

#### *PCI Address and Data*

Pin Names: PCI\_AD[31..0]

Pin Numbers: 72~74, 77~79, 82~83, 86~90, 93~95, 108~111, 114~115, 117~118, 120~121, 124~128, 1

Address and Data buses are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the first clock cycle in which PCI\_FRAME\_N signal is asserted. During the address phase, PCI\_AD[31:0] contain a physical address (32 bits). For I/O, this can be a byte address. For configuration and memory it is a DWORD address. During data phases, PCI\_AD[7:0] contain the least significant byte (LSB) and PCI\_AD[31:24] contain the most significant byte (MSB). Write data is stable and valid when PCI\_IRDY\_N is asserted; read data is stable and valid when PCI\_TRDY\_N is asserted. Data is transferred during those clocks where both PCI\_IRDY\_N and PCI\_TRDY\_N are asserted.

#### *PCI Command and Byte Enables*

Pin Names: PCI\_CBE[3..0]

Pin Numbers: 84, 96, 105, 119

Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, PCI\_CBE[3:0]\_N define the bus command. During the data phase, PCI\_CBE[3:0]\_N are used as Byte Enables. Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.

#### *PCI ID Select*

Pin Name: PCI\_IDSEL

Pin Number: 85

This signal is used as a chip select during configuration read and write transactions.

#### *PCI Frame Cycle*

Pin Name: PCI\_FRAME\_N

Pin Number: 97

Cycle Frame is driven by the current master to indicate the beginning and duration of an access. PCI\_FRAME\_N is asserted to indicate that a bus transaction is beginning. While PCI\_FRAME\_N is asserted, data transfers continue. When PCI\_FRAME\_N is de-asserted, the transaction is in the final data phase or has completed.

#### *PCI Initiator Ready*

Pin Name: PCI\_IRDY\_N

Pin Number: 98

Initiator Ready indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with PCI\_TRDY\_N. A data phase is completed on any clock when both PCI\_IRDY\_N and PCI\_TRDY\_N are sampled as asserted. Wait cycles are inserted until both PCI\_IRDY\_N and PCI\_TRDY\_N are asserted together.

#### *PCI Target Ready*

Pin Name: PCI\_TRDY\_N

Pin Number: 102

Target Ready indicates the target agent's ability to complete the current data phase of the transaction. PCI\_TRDY\_N is used with PCI\_IRDY\_N. A data phase is completed on any clock when both PCI\_TRDY\_N and PCI\_IRDY\_N are sampled asserted. During a read, PCI\_TRDY\_N indicates that valid data is present on PCI\_AD[31:0]. During a write, it indicates the target is prepared to accept data.

#### *PCI Device Select*

Silicon Image, Inc.

Pin Name: PCI\_DEVSEL\_N

Pin Number: 101

Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, PCI\_DEVSEL\_N indicates to a master whether any device on the bus has been selected.

#### *PCI Stop*

Pin Name: PCI\_STOP\_N

Pin Number: 100

PCI\_STOP\_N indicates the current target is requesting that the master stop the current transaction.

#### *PCI Parity Error*

Pin Name: PCI\_PERR\_N

Pin Number: 99

PCI\_PERR\_N indicates a data parity error between the current master and target on PCI. On a write transaction, the target always signals data parity errors back to the master on PCI\_PERR\_N. On a read transaction, the master asserts PCI\_PERR\_N to indicate to the system that an error was detected.

#### *PCI System Error*

Pin Name: PCI\_SERR\_N

Pin Number: 103

System Error is for reporting address parity errors, data parity errors on Special Cycle Command, or any other system error where the result will be catastrophic. The PCI\_SERR\_N is a pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of PCI\_SERR\_N is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of PCI\_SERR\_N to the de-asserted state is accomplished by a weak pull-up. Note that if an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

#### *PCI Parity*

Pin Name: PCI\_PAR

Pin Number: 104

PCI\_PAR is even parity across PCI\_AD[31:0] and PCI\_CBE[3:0]\_N. Parity generation is required by all PCI agents. PCI\_PAR is stable and valid one clock after the address phase. For data phases PCI\_PAR is stable and valid one clock after either PCI\_IRDY\_N is asserted on a write transaction or PCI\_TRDY\_N is asserted on a read transaction. Once PCI\_PAR is valid, it remains valid until one clock after the completion of the current data phase. (PCI\_PAR has the same timing as PCI\_AD[31:0] but delayed by one clock.)

#### *PCI Request*

Pin Name: PCI\_REQ\_N

Pin Number: 71

This signal indicates to the arbiter that this agent desires use of the PCI bus.

#### *PCI Grant*

Pin Name: PCI\_GNT\_N

Pin Number: 70

This signal indicates to the agent that access to the PCI bus has been granted. In response to a PCI request, this is a point-to-point signal. Every master has its own PCI\_GNT\_N, which must be ignored while PCI\_RST\_N is asserted.

#### *PCI Interrupt A*

Pin Name: PCI\_INTA\_N

Pin Number: 67

Interrupt A is used to request an interrupt on the PCI bus. PCI\_INTA\_N is open collector and is an open drain output.

#### *PCI Clock Signal*

Pin Names: PCI\_CLK

Pin Number: 69

Clock Signal provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals (except PCI\_RST\_N, and PCI\_INTA\_N) are sampled on the rising edge of PCI\_CLK. All other timing parameters are defined with respect to this edge.

#### *PCI Reset*

Pin Name: PCI\_RST\_N

Pin Number: 68

PCI\_RST\_N is an active low input that is used to set the internal registers to their initial state. PCI\_RST\_N is typically the system power-on reset signal as distributed on the PCI bus.

#### *PCI M66EN*

Pin Name: PCI\_M66EN

Pin Number: 116

This pin configures the PCI bus operating frequency. When low, the PCI bus operates from 0 to 33 MHz. When high, the PCI bus operates from 33MHz to 66MHz.

### **3.3.2 Miscellaneous I/O**

#### *Ground*

Pin Name: VSS

Pin Number: 41, 48, 76, 81, 92, 107, 113, and 123

Logic Ground. This ground pins are connected with GNDA (SerDes Ground) with an EPAD.

#### *TEST*

Pin Name: TEST\_MODE

Pin Number: 57

This pin is used, in conjunction with other pins, to enable various test functions within the device.

#### *Power Supply*

Pin Name(s): VDDO

Pin Number(s): 28, 40, 75, 91, 106, and 122

Power Supply Input

Pin Name(s): VDDI

Pin Number(s): 47, 80, and 112

Power Supply Input for internal core

#### *Internal Scan Test*

Pin Name: SCAN\_EN

Pin Number: 29

This pin, when active (high), will place all scan flip-flops into scan mode for chip testing. This pin must be left open or tied to ground for normal operation.

#### *LED Drivers*

Pin Names: LED[0..1]

Pin Numbers: 51, 66

These are 12mA open-drain outputs to drive Activity LEDs for IDE channels 0 and 1 respectively.

#### *Flash Signals*

Pin Name: FL\_ADDR[00] / IDE\_CFG

Pin Number: 31

When PCI\_RST\_N is deasserted, this pin is an output and represents flash memory address bit 0. During reset, it is sampled to configure Mass Storage class or RAID mode in the PCI Class Code register. A high on this pin sets Mass Storage class, a low sets RAID mode. The configuration state is latched internally when PCI\_RST\_N is deasserted. This pad is internally pulled high to enable Mass Storage class if left unconnected.

Pin Name: FL\_ADDR[01] / BA5\_EN

Pin Number: 32

When PCI\_RST\_N is deasserted, this pin is an output and represents flash memory address bit 1. During reset, it is sampled to configure Base address register 5. A high on this pin enables base address register 5, a low disables base address register 5. The configuration state is latched internally when PCI\_RST\_N is deasserted. This pin is internally pulled high to enable Base address register 5 when left unconnected.

Pin Name: FL\_ADDR[02-18]

Pin Numbers: 33, 36~39, 42~46, 49~50, 52~56

Flash Memory address bits; 19 total for 512K address space. Flash address pins 15 to 18 are used to select internal test modes in conjunction with the TEST\_MODE pin; they have internal pull-downs and must be unconnected or pulled down.

Pin Name: FL\_DATA[00-07]

Pin Numbers: 58~65

8-bit Flash memory data bus.

Pin Name: FL\_RD\_N

Pin Number: 35

Flash read enable signal, active low

Pin Name: FL\_WR\_N

Pin Number: 34

Flash write enable signal, active low

#### *Memory Chip Select*

Pin Name: MEM\_CS\_N

Pin Number: 30

This pin is used to select and enable the external memory. It is active low.

#### *Serial Interface Signals*

Pin Name: EEPROM\_SDAT

Pin Number: 2

Serial Interface data line

Pin Name: EEPROM\_SCLK

Pin Number: 3

Serial Interface clock

### **3.3.3 Serial ATA Signals**

#### *Power Supply & Ground*

Pin Name: VDDA

Pin Numbers: 4, 8, 13, 17

SerDes 1.8 V Power supply Pins

Pin Name: VDDP

Pin Numbers: 22, 23

PLL 1.8 V Power supply Pins

Pin Name: GNDA

Pin Numbers: 7, 9, 12, 16, 18, 21, and 25

SerDes Ground. This ground pins are connected with VSS (Logic Ground) with an EPAD.

*High Speed Serial Signals*

Pin Name: RxN1  
Pin Number: 15  
Channel 1 high-speed differential receive negative side.

Pin Name: RxP1  
Pin Number: 14  
Channel 1 high-speed differential receive positive side. Loading an internal register through the flash or EEPROM during the initialization sequence could reverse RxP1 and RxN1 pinouts.

Pin Name: TxN1  
Pin Number: 19  
Channel 1 high speed differential transmit negative side

Pin Name: TxP1  
Pin Number: 20  
Channel 1 high speed differential transmit positive side

Pin Name: RxN2  
Pin Number: 6  
Channel 2 high-speed differential receive negative side.

Pin Name: RxP2  
Pin Number: 5  
Channel 2 high-speed differential receive positive side. Loading an internal register through the flash or EEPROM during the initialization sequence could reverse RxP2 and RxN2 pinouts.

Pin Name: TxN2  
Pin Number: 10  
Channel 2 high speed differential transmit negative side

Pin Name: TxP2  
Pin Number: 11  
Channel 2 high speed differential transmit positive side

*Other SerDes Signals*

Pin Name: XTALO  
Pin Number: 27  
Crystal oscillator pin for SerDes reference clock. A 25MHz crystal must be used.

Pin Name: XTALI/CLKI  
Pin Number: 26  
Crystal oscillator pin for SerDes reference clock. When external clock source is selected, the external clock (either 25MHz or 100 MHz) will come in through this pin. The clock precision requirement is  $\pm 100$ ppm.

Pin Name: REXT  
Pin Number: 24  
External reference resistor pin for termination calibration. This pin provides the addition function of selecting frequency of the clock source . For 25MHz crystal/external clock, a 1K, 1% resistor is connected to ground. To use 100MHz external clock, a 4.99K, 1% resistor is connected to ground.



## 4 Package Drawing

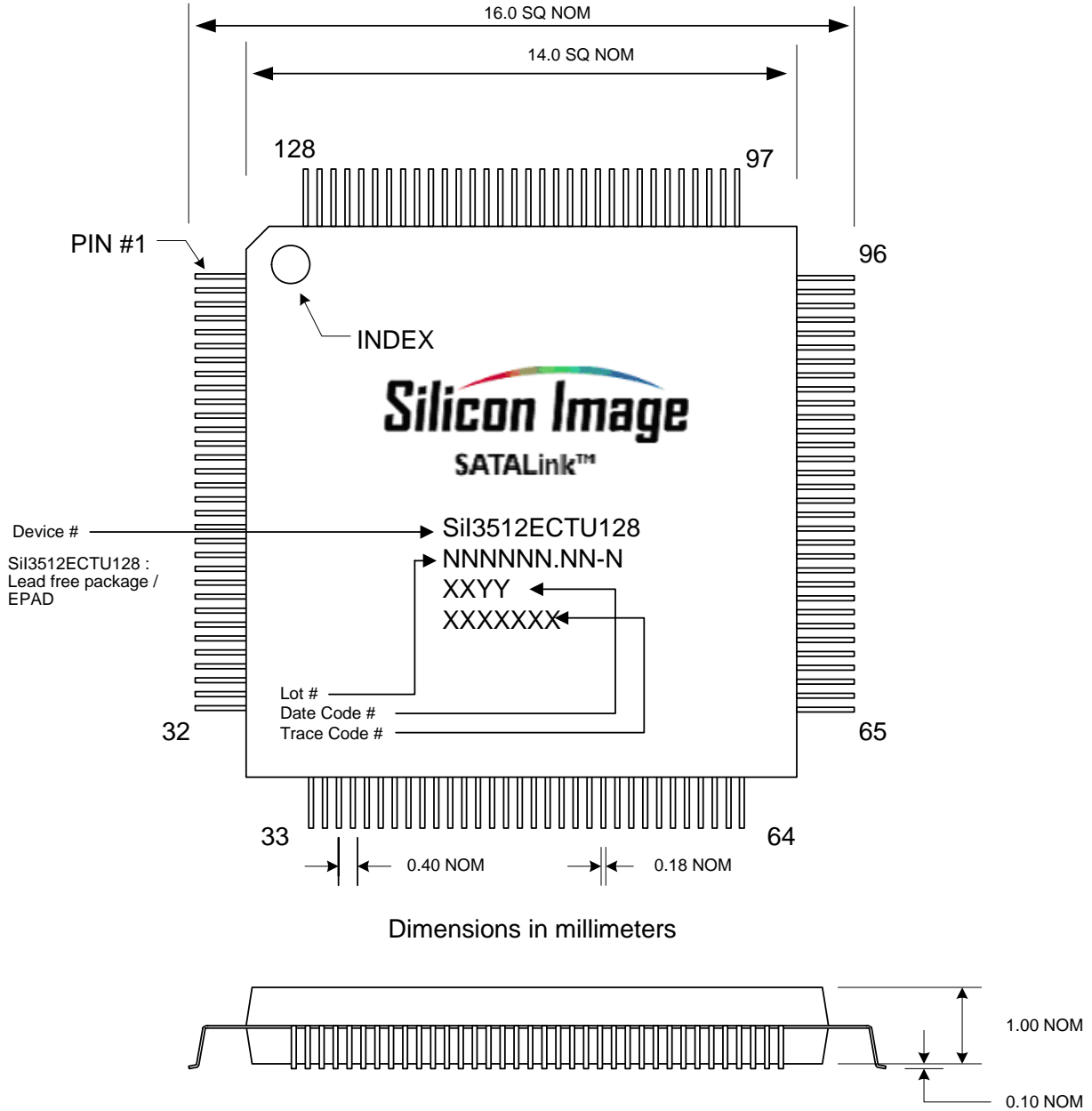


Figure 4-1: Package Drawing – 128 TQFP

Part Ordering Number:  
SiI3512ECTU128 (128 pin TQFP lead free package with an exposed pad)

## 5 Enhanced Packaging (Sil3512ECTU128)

The Sil3512ECTU128 is packaged in a 128 pin TQFP with an exposed metal pad (5.385mm x 5.385mm) on the package designed to improve signal quality by having a low inductance ground connection. The exposed pad should be soldered to a landing area on the PCB, as described below. The characterization results show improved signal quality by going above 25% coverage of the exposed pad area. A poor connection of the exposed pad to the landing area on the PCB may result in CRC or primitive error if the environments are noisy.

### 5.1 PCB Design Requirements

In order to improve the signal quality, it is required that landing area be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad on the package, as shown in Figure 3 (TQFP Landing area Design on PCB). Although the size of this landing area can be larger than the exposed pad on the package, the solderable area, as defined by the solder mask, should be at least the same as the exposed pad area on the package. A clearance of at least 0.5 mm should be designed on the PCB between the outer edges of the landing area and the inner edges of pad pattern for the leads to avoid any shorts.

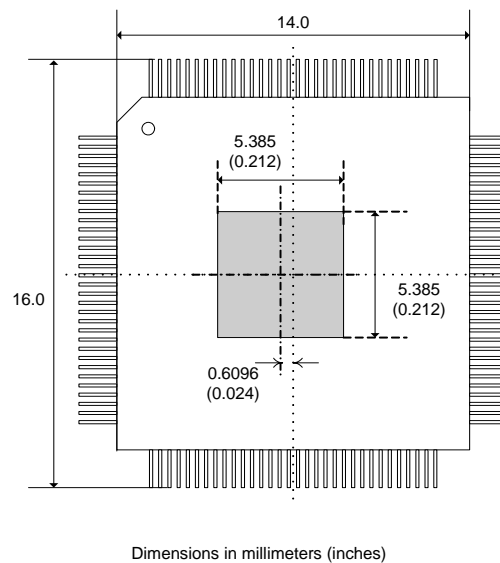
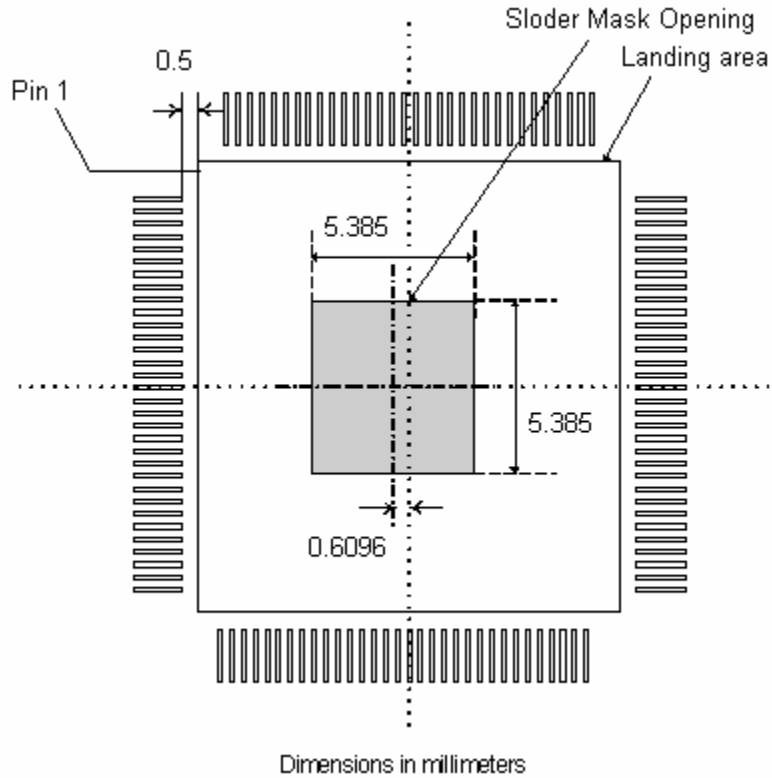
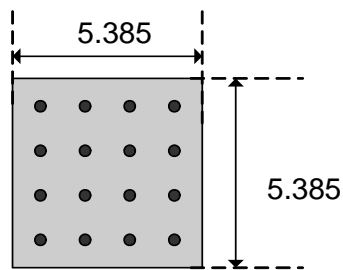


Figure 5-1: Top View of Enhanced 128-pin TQFP Package



**Figure 5-2: Top View of TQFP Landing area Design on PCB**

Ground vias are required in the metal land to provide a low impedance connection to ground. An array of vias should be incorporated in the ground pad at a 1.2 mm pitch grid, as shown in Figure 4 (Ground Pad Via Grid). The via diameter should be approximately 0.30mm (12mils). It is also desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad and the PCB landing area. The ground vias can be “tented” with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 0.1 mm (4 mils) larger than the via diameter.



0.3 mm diameter with 1.2 mm pitch Ground Via

Dimensions in millimeters

**Figure 5-3: Ground Pad Via Grid**

### Board Mounting Guidelines

The following are general recommendations for mounting exposed pad leadframe devices on the PCB. This should serve as the starting point in assembly process development and it is recommended that the process should be developed based on past experience in mounting standard, non-epad packages.

### Stencil Design:

For proper ground connection, it is required that the exposed pad on the package be soldered to the landing area on the PCB. This requires solder paste application not only on the pad pattern for lead attachment but also on the landing area using the stencil. While for standard (non-epad) leadframe based packages the stencil thickness depends on the lead pitch and package coplanarity only, the package standoff also needs to be considered for the ground enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1 mm, the stencil thickness of 5 to 8 mils (depending upon the pitch) should still provide good solder joint between the exposed pad and the landing area. The aperture openings should be the same as the solder mask opening on the ground land. Since a large stencil opening may result in poor release, the aperture opening can be subdivided into an array of smaller openings, similar to the ground land pattern shown in Figure 5. Recommended Stencil Design. The above guidelines will result in the solder joint area to be about 80 to 90% of the exposed pad area.

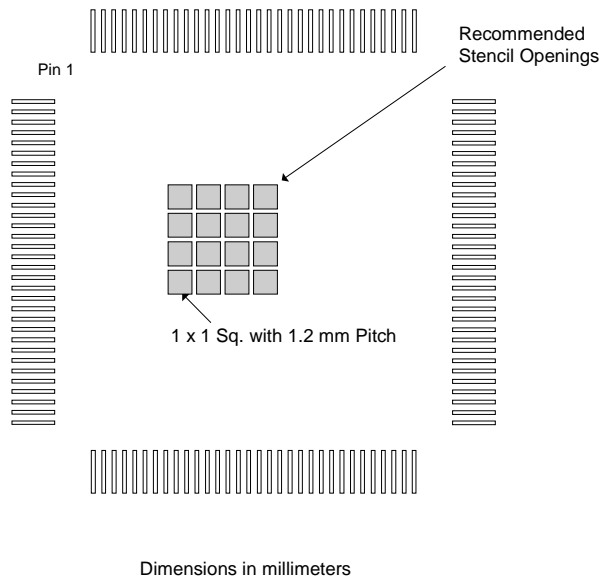


Figure 5-4: Top View of Recommended Stencil Design

## 6 Block Diagram

The Sil3512 contains the major logic modules shown below.

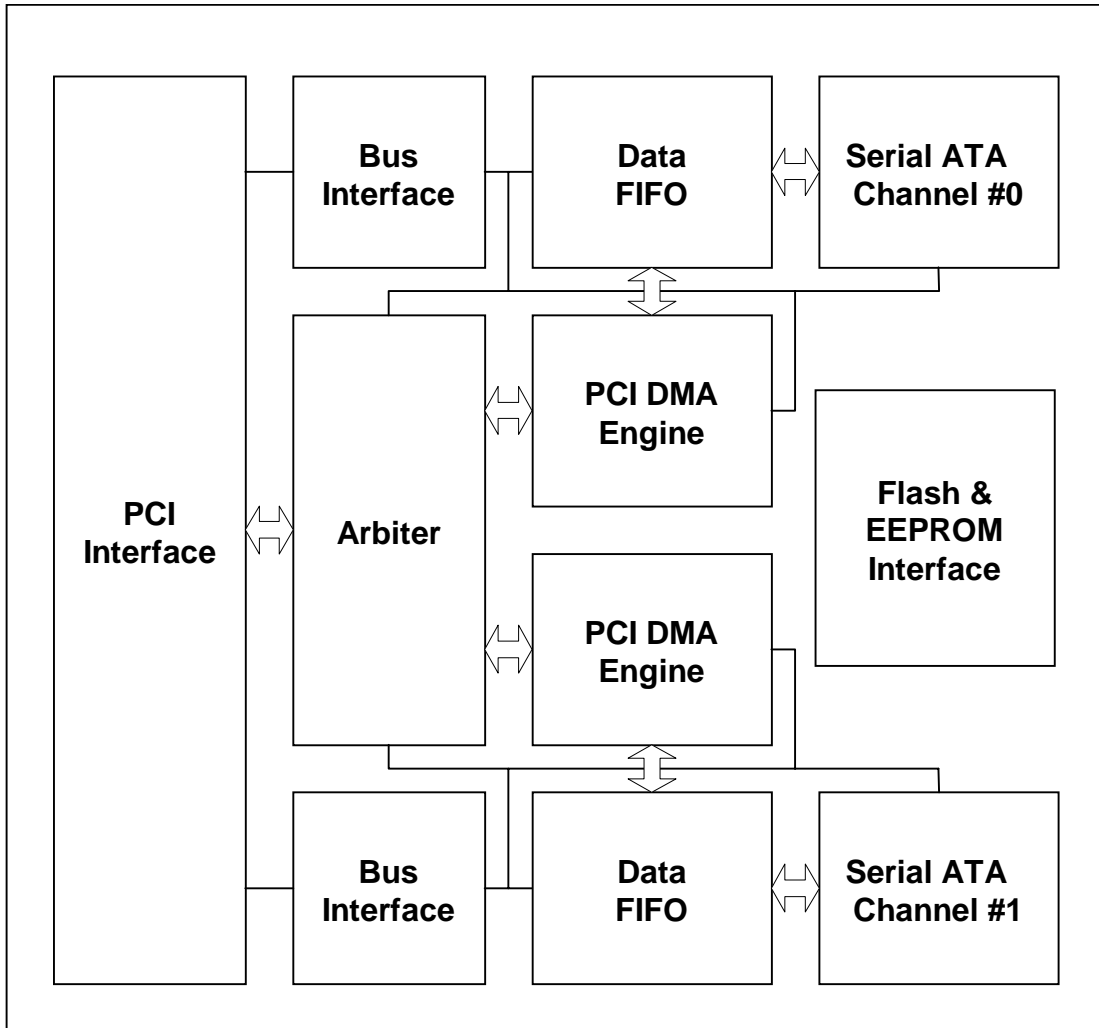


Figure 6-1: Sil3512 Block Diagram

## 7 Auto-Initialization

The Sil3512 supports an external FLASH and/or EEPROM device for BIOS extensions and user-defined PCI configuration header data.

### 7.1 Auto-Initialization from FLASH

The Sil3512 initiates the FLASH detection and configuration space loading sequence upon the release of PCI\_RST\_N. It begins by reading the highest two addresses (7FFFF<sub>H</sub> and 7FFFE<sub>H</sub>), checking for the correct data signature pattern – AA<sub>H</sub> and 55<sub>H</sub>, respectively. If the data signature pattern is correct, the Sil3512 continues to sequence the address downward, reading a total of sixteen bytes. If the Data Signature is correct (55<sub>H</sub> at 7FFFC<sub>H</sub>), the last twelve bytes are loaded into the PCI Configuration Space registers.

Note: If both Flash and EEPROM are installed, the PCI Configuration Space registers will be loaded with EEPROM's data. While the sequence is active, the Sil3512 responds to all PCI bus accesses with a Target Retry.

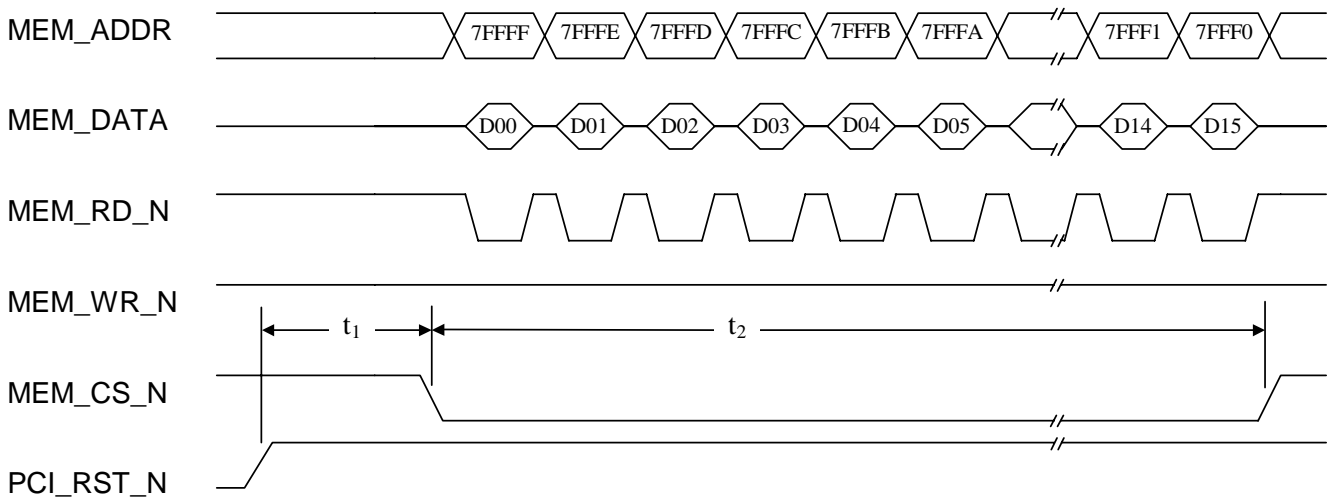


Figure 7-1 Auto-Initialization from Flash Timing

Parameter	Value	Description
t <sub>1</sub>	660 ns	PCI reset to Flash Auto-Initialization cycle begin
t <sub>2</sub>	9600 ns	Flash Auto-Initialization cycle time

Table 7-1 Auto-Initialization from Flash Timing

Address	Data Byte	Description
7FFFF <sub>H</sub>	D00	Data Signature = AA <sub>H</sub>
7FFFE <sub>H</sub>	D01	Data Signature = 55 <sub>H</sub>
7FFFD <sub>H</sub>	D02	AA = 120 ns FLASH device / Else, 240 ns FLASH device
7FFFC <sub>H</sub>	D03	Data Signature = 55 <sub>H</sub>
7FFFB <sub>H</sub>	D04	PCI Device ID [23:16]
7FFFA <sub>H</sub>	D05	PCI Device ID [31:24]
7FFF9 <sub>H</sub>	D06	PCI Class Code [15:08]
7FFF8 <sub>H</sub>	D07	PCI Class Code [23:16]
7FFF7 <sub>H</sub>	D08	PCI Sub-System Vendor ID [07:00]
7FFF6 <sub>H</sub>	D09	PCI Sub-System Vendor ID [15:08]
7FFF5 <sub>H</sub>	D10	PCI Sub-System ID [23:16]
7FFF4 <sub>H</sub>	D11	PCI Sub-System ID [31:24]
7FFF3 <sub>H</sub>	D12	SerialATA PHY Config [07:00]
7FFF2 <sub>H</sub>	D13	SerialATA PHY Config [15:08]
7FFF1 <sub>H</sub>	D14	SerialATA PHY Config [23:16]
7FFF0 <sub>H</sub>	D15	SerialATA PHY Config [31:24]

Table 7-2 Flash Data Description

## 7.2 Auto-Initialization from EEPROM

The Sil3512 initiates the EEPROM detection and configuration space loading sequence after the FLASH read sequence. The Sil3512 supports up to 256 byte EEPROM with a 2-wire serial interface. The sequence of operations consists of the following.

- 1) START condition defined as a high-to-low transition on SDAT while SCLK is high.
- 2) Control byte = 1010 (Control Code) + 000 (Chip Select) + 0 (Write Address)
- 3) Acknowledge
- 4) Starting address field = 00000000.
- 5) Acknowledge
- 6) Sequential data bytes separated by Acknowledges.
- 7) STOP condition.

While the sequence is active, the Sil3512 responds to all PCI bus accesses with a Target Retry.

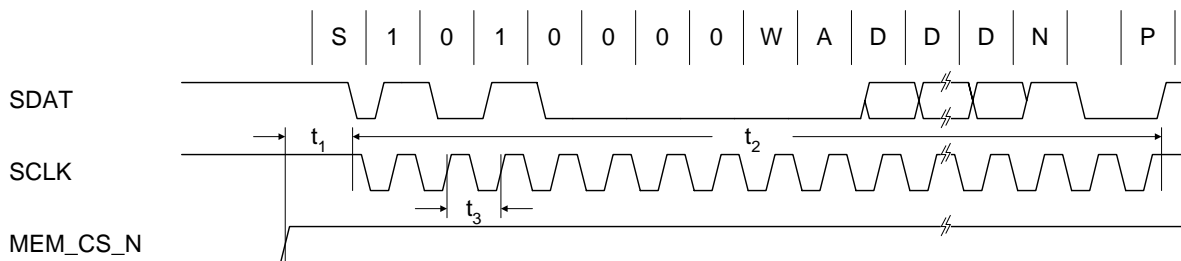


Figure 7-2 Auto-Initialization from EEPROM Timing

Parameter	Value	Description
$t_1$	26.00 $\mu$ s	End of Auto-Initialization from FLASH to start of Auto-Initialization from EEPROM
$t_2$	2.66 ms	Auto-Initialization from EEPROM cycle time
$t_3$	19.26 $\mu$ s	EEPROM serial clock period

**Table 7-3 Auto-Initialization from EEPROM Timing**

Parameter	Description
S	START condition
W	R/W 0 = Write Command, 1 = Read Command
A	Acknowledge
D	Serial data
N	No-Acknowledge
P	STOP condition

**Table 7-4 Auto-Initialization from EEPROM Timing Symbols**

Address	Data Byte	Description
00 <sub>H</sub>	D00	Memory Present Pattern = AA <sub>H</sub>
01 <sub>H</sub>	D01	Memory Present Pattern = 55 <sub>H</sub>
02 <sub>H</sub>	D02	Data Signature = AA <sub>H</sub>
03 <sub>H</sub>	D03	Data Signature = 55 <sub>H</sub>
04 <sub>H</sub>	D04	PCI Device ID [23:16]
05 <sub>H</sub>	D05	PCI Device ID [31:24]
06 <sub>H</sub>	D06	PCI Class Code [15:08]
07 <sub>H</sub>	D07	PCI Class Code [23:16]
08 <sub>H</sub>	D08	PCI Sub-System Vendor ID [07:00]
09 <sub>H</sub>	D09	PCI Sub-System Vendor ID [15:08]
0A <sub>H</sub>	D10	PCI Sub-System ID [23:16]
0B <sub>H</sub>	D11	PCI Sub-System ID [31:24]
0C <sub>H</sub>	D12	SerialATA PHY Config [07:00]
0D <sub>H</sub>	D13	SerialATA PHY Config [15:08]
0E <sub>H</sub>	D14	SerialATA PHY Config [23:16]
0F <sub>H</sub>	D15	SerialATA PHY Config [31:24]

**Table 7-5 EEPROM Data Description**



## 8 ATA Command Supported

### 8.1 Data Modes

The Sil3512 PCI to Serial ATA Controller has an internal datapath interface between the PCI block and the Serial ATA controller block. The data modes (Register mode, PIO mode and DMA mode) are of no significance inside the Sil3512.

### 8.2 ATA Commands

The Sil3512 PCI to Serial ATA Controller decodes ATA commands in hardware. The commands supported include ATA/ATAPI-5 and ATA/ATAPI-6 commands, including the 48-bit LBA extended commands. Certain obsolesced commands are also supported. The supported commands are listed below:

**Table 8-1 Supported ATA Commands**

Command	Command/ Features Codes	Comment
CFA Erase Sectors	C0h	
CFA Request Extended Error Code	03h	
CFA Translate Sector	87h	
CFA Write Multiple without Erase	CDh	
CFA Write Sectors without Erase	38h	
Check Media Card Type	D1h	
Check Power Mode	E5h	
Configure Stream	51h	
Device Configuration Freeze Lock	B1h/C1h	
Device Configuration Identify	B1h/C2h	
Device Configuration Restore	B1h/C0h	
Device Configuration Set	B1h/C3h	
Device Reset	08h	
Download Microcode	92h	
Execute Device Diagnostics	90h	The two Serial ATA ports for Sil3512 PCI to Serial ATA Controller are both "single masters".
Flush Cache	E7h	
Flush Cache Ext	EAh	48-bit LBA Command
Format Track	50h	Obsolesced vendor specific command, needs to be programmed as vendor specific commands
Get Media Status	DAh	
Identify Device	ECh	
Identify Packet Device	A1h	
Idle	E3h	

Command	Command/ Features Codes	Comment
Idle Immediate	E1h	
Initialize Device Parameters	91h	Obsolesced in ATA/ATAPI-6.
Media Eject	EDh	
Media Lock	DEh	
Media Unlock	DFh	
Nop	00h	
Packet	A0h	
Read Buffer	E4h	
Read DMA	C8h	
	C9h	Obsolesced Command code supported, decoded as Command Code C8h
Read DMA Ext	25h	48-bit LBA Command
Read DMA Queued	C7h	
Read DMA Queued Ext	26h	48-bit LBA Command
Read Log Ext	2Fh	
Read Long	22h	Obsolesced command
	23h	
Read Multiple	C4h	
Read Multiple Ext	29h	48-bit LBA Command
Read Native Max Address	F8h	
Read Native Max Address Ext	27h	48-bit LBA Command
Read Sector(s)	20h	
	21h	Obsolesced Command code supported, decoded as Command Code 20h
Read Sector(s) Ext	24h	48-bit LBA Command
Read Stream DMA	2A	
Read Stream PIO	2B	
Read Verify Sector(s)	40h	
	41h	Obsolesced Command code supported, decoded as Command Code 40h
Read Verify Sector(s) Ext	42h	48-bit LBA Command
ReadFPDMAQueued	2Ch	
Recalibrate	10h	Obsolesced command supported.
Security Disable Password	F6h	
Security Erase Prepare	F3h	
Security Erase Unit	F4h	

Command	Command/ Features Codes	Comment
Security Freeze Lock	F5h	
Security Set Password	F1h	
Security Unlock	F2h	
Seek	70h	
Service	A2h	
Set Features	EFh	
Set Max Address	F9h/00h	
Set Max Address Ext	37h	48-bit LBA Command
Set Max Freeze Lock	F9h/04h	
Set Max Lock	F9h/02h	
Set Max Unlock	F9h/03h	Obsolesced command supported.
Set Max Set Password	F9h/01h	
Set Multiple Mode	C6h	The Sil3512 PCI to Serial ATA Controller intercepts the command to set up the number of sectors for a DRQ block upon this command.
Sleep	E6h	
Smart Disable Operations	B0h/D9h	
Smart Enable Operations	B0h/D8h	
Smart Enable/Disable Attributes Autosave	B0h/D2h	
Smart Execute Off-Line Immediate	B0h/D4h	
Smart Read Attribute Thresholds	B0h/D1h	Obsolesced command supported.
Smart Read Data	B0h/D0h	
Smart Read Log	B0h/D5h	
Smart Return Status	B0h/DAh	
Smart Save Attribute Values	B0h/D3h	Obsolesced command supported.
Smart Write Log	B0h/D6h	
Standby	E2h	
Standby Immediate	E0h	
Write Buffer	E8h	
Write DMA	CAh	
	CBh	Obsolesced Command code supported, decoded as Command Code CAh
Write DMA Ext	35h	48-bit LBA Command
Write DMA Queued	CCh	
Write DMA Queued Ext	36h	48-bit LBA Command
Write Log Ext	3Fh	
Write Long	32h	Obsolesced command supported

Command	Command/ Features Codes	Comment
	33h	
Write Multiple	C5h	
Write Multiple Ext	39h	48-bit LBA Command
Write Sector(s)	30h	
	31h	Obsolesced Command code supported, decoded as Command Code 30h
Write Sector(s) Ext	34h	48-bit LBA Command
Write Stream DMA	3Ah	
Write Stream PIO	3Bh	
WriteFPDMAQueued	3Ch	

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