Sil3132

PCI Express to Serial ATA Controller

Data Sheet

Document # **SiI-DS-0136**-B

-

Aug 2006

Revision History

Revision	Comment	Date
A	Derived from preliminary datasheet rev 0.3	04/08/05
A1	Corrected inconsistent sentences (minor fixes including mistyping)	08/11/06
B	Updated Company Logo	08/14/06

Table of Contents

Table of Tables

Table of Figures

1 Overview

The Silicon Image SiI3132 is a two-port PCI Express to Serial ATA controller. The SiI3132 is designed to provide multiple port serial ATA connectivity with minimal host overhead and host to device latency. The SiI3132 supports a 1-lane 2.5 Gb/s PCI Express bus and the Serial ATA Generation 2 transfer rate of 3.0 Gb/s (300 MB/s).

1.1 Features

1.1.1 Overall Features

- Host Protocol
  - Optimized for transaction oriented designs – minimal Host overhead
  - Supports two command issuance mechanisms
    - Efficient in both embedded and PC implementations
    - Reduces dependency on bridge behavior
- Supports up to 4Mbit external Flash for BIOS expansion
- Supports a master/slave I^2C interface
- Supports external Flash or serial EEPROM for programmable subsystem vendor ID / subsystem product ID
- Fabricated in a 0.18µ CMOS process with a 1.8 volt core and 3.3 volt I/Os
- Available in an 88-pin QFN package (10x10 mm, 0.4 mm lead pitch). **An EPAD must be soldered to PCB GND**
- JTAG boundary scan

1.1.2 PCI Express Features

- Supports 1-lane 2.5 Gb/s PCI Express
- Internal application interface multiplexed to 2 ports
- All registers appear in unified memory space
- All registers accessible through I/O space
- Full-chip command completion status accessible with single PCI Express access

1.1.3 Serial ATA Features

- Integrated Serial ATA Link and PHY logic
- Compliant with Serial ATA 1.0 specifications
- Supports Serial ATA Generation 2 transfer rate of 3.0 Gb/s
- Plesiochronous, Single PLL architecture, 1 PLL for 2 ports
- Output Swing Control
- Supports two independent Serial ATA channels
  - Independent Link, Transport, and data FIFO
  - Independent command fetch, scatter/gather, and command execution
    - Hard coded state machines – no code space or download
  - Supports Legacy Command Queuing (LCQ)
  - Supports Native Command Queuing (NCQ)
  - Supports Non-zero offsets NCQ
  - Supports Out of order data delivery NCQ
  - Supports FIS-based switching with Port Multipliers
- 31 Commands and Scatter/Gather Tables per Port on-chip
- Protocol Override per Command
- Staggered Spin-up Control

1.2 References

- Serial ATA / High Speed Serialized AT Attachment specification, Revision 1.0
- PCI Express Base Specification Revision 1.0a

2 Electrical Characteristics

2.1 Device Electrical Characteristics

Specifications are for Commercial Temperature range, 0°C to +70°C, unless otherwise specified.

Symbol	Parameter	Ratings	Unit
VDDO	I/O Supply Voltage	4.0	V
VDDD	Core Supply Voltage	2.15	V
VDDSRX, VDDSTX VDDSPLL, VDDPRX VDDPTX, VDDPTXPLL VDDPRXPLL, VDDX	Supply Voltage for S-ATA and PCI Exp Receivers, Transmitters, and PLLs, respectively	2.15	V
V_{IN}	Input Voltage	-0.3 ~ VDD+0.3	V
I_{OUT}	DC Output Current	16	mA
θ_{JA}	Thermal Resistance, Junction to Ambient, Still Air	22.2[1]	°C/W
T_{STG}	Storage Temperature	-65 ~ 150	°C

Notes: [1] An EPAD must be soldered to PCB GND

Table 2-1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Type	Limits			Unit
				Min	Typ	Max	
VDDD	Core Supply Voltage	-	-	1.71	1.8	1.89	V
VDDSRX	S-ATA Receiver Supply Voltage	-	-				
VDDSTX	S-ATA Transmitter Supply Voltage	-	-				
VDDSPLL	S-ATA SerDes PLL Supply Voltage	-	-				
VDDPRX	PCI Exp Receiver Supply Voltage	-	-				
VDDPTX	PCI Exp Transmitter Supply Voltage	-	-				
VDDPTX PLL	PCI Exp Transmitter PLL Supply Voltage	-	-				
VDDPRX PLL	PCI Exp Receiver PLL Supply Voltage	-	-				
VDDX	Oscillator Supply Voltage	-	-				
VDDO	Supply Voltage(I/O)	-	-	3.0	3.3	3.6	V
$IDD_{1.8V-3G}$	Supply Current (1.8V Supply)	3GHz Operating	-	-	450	570	mA
$IDD_{1.8V-1.5G}$	Supply Current (1.8V Supply)	1.5GHz Operating	-	-	380	500	mA
V_{IH}	Input High Voltage	3.3V I/O		2.0	-	-	V
V_{IL}	Input Low Voltage	3.3V I/O				0.8	V
V+	Input High Voltage	3.3V I/O	Schmitt	-	1.8	2.3	V
V-	Input Low Voltage	3.3V I/O	Schmitt	0.5	0.9	-	V
V_H	Hysteresis Voltage	3.3V I/O	Schmitt	0.4	-	-	V
I_{IH}	Input High Current	V_{IN} = VDD	-	-10	-	10	µA
I_{IL}	Input Low Current	V_{IN} = VSS	-	-10	-	10	µA
V_{OH}	Output High Voltage	-	-	2.4	-	-	V
V_{OL}	Output Low Voltage	-	-	-	-	0.4	V
I_{OZ}	3-State Leakage Current	-	-	-10	-	10	µA

3.3V power consumption depends on LED, JTAG, Enclosure management status. If all are disabled, 3.3V power consumption will be uA.

Table 2-2 DC Specifications

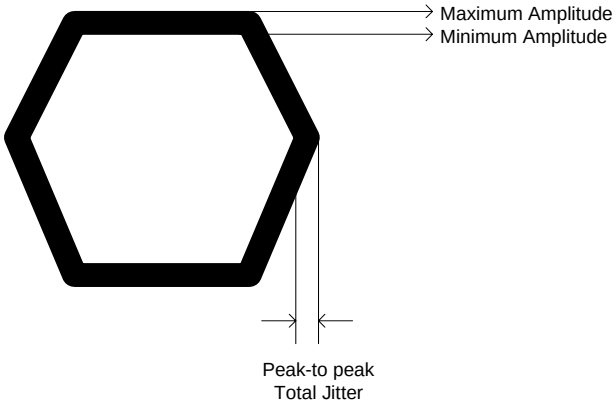
Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{SATA_DOUT}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. BAR1 1050h [4:0] = 0x0C[1]	400	550	700	mV
V_{SATA_DIN}	RX+/RX- differential peak-to-peak input sensitivity		240			mV
V_{SATA_SQ}	RX+/RX- OOB Signal Detection Threshold		50	125	240	mV
V_{SATA_ACCM}	Tx AC common-mode voltage				50	mV
Z_{SATA_DIN}	Tx Pair Differential impedance		85	100	115	ohms
Z_{SATA_DOUT}	Rx Pair Differential impedance		85	100	115	ohms
Z_{SATA_SIN}	Tx Single-Ended impedance		40			ohms
Z_{SATA_SOUT}	Rx Single-Ended impedance		40			ohms

Notes: [1] 0x0C is a reset value.

Table 2-3 SATA Interface DC Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{PCI_DOUT}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms.	800	1000	1200	mV
$V_{PCI\_DE\text{-}RATIO}$	Tx De-Emphasized Differential Output Voltage	Ratio	- 3.0	-3.5	-4.0	dB
V_{PCI_DIN}	RX+/RX- differential peak-to-peak input sensitivity		175		1200	mV
Z_{PCI_DIN}	Tx Pair Differential impedance	DC impedance	80	100	120	ohms
Z_{PCI_DOUT}	Rx Pair Differential impedance	DC impedance	80	100	120	ohms
Z_{PCI_SIN}	Tx Single-Ended impedance	DC impedance	40	50	60	ohms
Z_{PCI_SOUT}	Rx Single-Ended impedance	DC impedance	40	50	60	ohms
$Z_{PCI\_RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Rx Powered Down Impedance	DC impedance	200k			ohms
$Z_{PCI\_RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Electtical Idle Detect Threshold	Measured at the Rx pins	65		175	mV

Table 2-4 PCI Express Interface DC Specifications



Eye Diagram

2.2 SATA Interface Timing Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
$T_{TX\_RISE\_FALL}$	Rise and Fall time at transmitter	20%-80% at Gen 1 20%-80% at Gen 2	100 67		273 136	ps
$T_{TX\_TOL\_FREQ}$	Tx Frequecny Long Term Stability		-350		+350	ppm
$T_{TX\_AC\_FREQ}$	Tx Spread-Sprectrum Modulation Deviation	CLKI = SSC AC modulation, subject to the "Downspread SSC" triangular modulation (30-33KHz) profile per 6.6.4.5 in SATA 1.0 specification	-5000		+0	ppm
T_{TX_SKEW}	Tx Differential Skew				15	ps

Table 2-5 SATA Interface Timing Specifications

2.3 SATA Interface Transmitter Output Jitter Characteristics

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
TJ_{5UI_15G}	Total Jitter, Data-Data 5UI	Measured at Tx output pins peak to peak phase variation Random data pattern		80		ps
DJ_{5UI_15G}	Deterministic Jitter, Data-Data 5UI	Measured at Tx output pins peak to peak phase variation Random data pattern		40		ps
TJ_{250UI_15G}	Total Jitter, Data-Data 250UI	Measured at Tx output pins peak to peak phase variation Random data pattern		100		ps
DJ_{250UI_15G}	Deterministic Jitter, Data-Data 250UI	Measured at Tx output pins peak to peak phase variation Random data pattern		60		ps

Table 2-6 SATA Interface Transmitter Output Jitter Characteristics, 1.5 Gb/s

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
$TJ_{fBAND/10\_3G}$	Total Jitter, $f_{C3dB}=f_{BAUD}/10$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		60		ps
$DJ_{fBAND/10\_3G}$	Deterministic Jitter, $f_{C3dB}=f_{BAUD}/10$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		15		ps
$TJ_{fBAND/500\_3G}$	Total Jitter, $f_{C3dB}=f_{BAUD}/500$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		70		ps
$DJ_{fBAND/500\_3G}$	Deterministic Jitter, $f_{C3dB}=f_{BAUD}/500$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		20		ps

Table 2-7 SATA Interface Transmitter Output Jitter Characteristics, 3 Gb/s

2.4 PCI Express Interface Timing Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
T_{PCI_UI}	Tx / Rx Unit Interval	SSC disabled	399.88	400	400.12	ps
$T_{PCI\_TX\_RISE\_FALL}$	Rise and Fall time at transmitter	20%-80%	0.125			UI
$T_{PCI\_TX-IDLE-MIN}$	Minimum time spent in Electrical Idle		50			UI
$T_{PCI\_TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered set				20	UI
$T_{PCI\_TX-IDLE-TO-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Elctrical Idle condition				20	UI
T_{PVPERL}	Power stable to PERST# inactive		100			ms
$T_{PERST-CLK}$	REFCLK stable before PERST# inactive		100			us
T_{PERST}	PERST# active time		100			us

Table 2-8 PCI Express Interface Timing Specifications

2.5 PCI Express Interface Transmitter Output Jitter Characteristics

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
TJ_{PCIe}	Total Jitter	Defined by PCI Express Base Specification Rev 1.1		65		ps

Table 2-9 PCI Express Interface Transmitter Output Jitter Characteristics

2.6 CLKI SATA Reference Clock Input Requirements

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
T_{CLKI_FREQ}	Nominal Frequency			25		MHz
V_{CLKI_IH}	Input High Voltage	-	0.7xVDDX			V
V_{CLKI_IL}	Input Low Voltage	-			0.3xVDDX	V
T_{CLKI_J}	CLKI frequency tolerance	-	-50		+50	ppm
$T_{CLKI\_RISE\_FALL}$	Rise and Fall time at CLKI	25MHz reference			4	ns
T_{CLKI_RJ}	Random Jitter	Measured at CLKI pin 10^{-12} Bit Error Ratio 1 sigma deviation			50	psrms
T_{CLKI_TJ}	Total Jitter	Measured at CLKI pin 10^{-12} Bit Error Ratio peak-to-peak phase noise			1	ns
$T_{CLKI\_RC\_DUTY}$	CLKI duty cycle	20%-80%	40		60	%

Table 2-10 CLKI SerDes Reference Clock Input Requirements

2.7 Power Supply Noise Requirements

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{NOISE_VDDA}	1.8V Analog Power Noise	peak-to-peak sinewave across 500KHz to 3GHz frequency range. Measured with differential probe trigger by nois source			50	mV
V_{NOISE_VDDD}	1.8V Digital Power Noise				100	mV
V_{NOISE_VDDO}	3.3V IO Power Noise				200	mV

Table 2-11 Power Supply Noise Requirements

3 Pin Definition

3.1 SiI3132 Pin Listing

This section describes the pin-out of the SiI3132 PCI Express to Serial ATA host controller. The table below gives the pin numbers, pin names, pin types, drive types where applicable, internal resistors where applicable, and descriptions. Power pins (VDD and VSS) are excluded from this listing.

Table 3-1 SiI3132 Pin Listing

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
4	RX1+	Diff In			Serial port 1 differential receiver + input
5	RX1-	Diff In			Serial port 1 differential receiver – input
8	TX1-	Diff Out			Serial port 1 differential transmitter – output
9	TX1+	Diff Out			Serial port 1 differential transmitter + output
13	TX0+	Diff Out			Serial port 0 differential transmitter + output
14	TX0-	Diff Out			Serial port 0 differential transmitter – output
17	RX0-	Diff In			Serial port 0 differential receiver – input
18	RX0+	Diff In			Serial port 0 differential receiver + input
20	REFCLK+	Diff In			PCI Express differential reference clock + input
21	REFCLK-	Diff In			PCI Express differential reference clock - input
25	PRX+	Diff In			PCI Express differential receiver + input
26	PRX-	Diff In			PCI Express differential receiver – input
29	PTX-	Diff Out			PCI Express differential transmitter – output
30	PTX+	Diff Out			PCI Express differential transmitter + output
34	PERST_N	I-Schmitt			PCI Express Reset
36	LED1	OD	12 mA		Channel 1 activity LED indicator
37	LED0	OD	12 mA		Channel 0 activity LED indicator
39	FL_DATA0	I/O	8 mA	PU-70K	Flash Memory Data 0
40	FL_DATA1	I/O	8 mA	PU-70K	Flash Memory Data 1
41	FL_DATA2	I/O	8 mA	PU-70K	Flash Memory Data 2
42	FL_DATA3	I/O	8 mA	PU-70K	Flash Memory Data 3
43	FL_DATA4	I/O	8 mA	PU-70K	Flash Memory Data 4
45	FL_DATA5	I/O	8 mA	PU-70K	Flash Memory Data 5
46	FL_DATA6	I/O	8 mA	PU-70K	Flash Memory Data 6
47	FL_DATA7	I/O	8 mA	PU-70K	Flash Memory Data 7
49	FL_ADDR00	I/O	8 mA	PU-70K	Flash Memory Address 0
50	FL_ADDR01	I/O	8 mA	PU-70K	Flash Memory Address 1
51	FL_ADDR02	I/O	8 mA	PU-70K	Flash Memory Address 2
52	FL_ADDR03	I/O	8 mA	PU-70K	Flash Memory Address 3
53	FL_ADDR04	I/O	8 mA	PU-70K	Flash Memory Address 4
55	FL_ADDR05	I/O	8 mA	PU-70K	Flash Memory Address 5
56	FL_ADDR06	I/O	8 mA	PU-70K	Flash Memory Address 6
57	FL_ADDR07	I/O	8 mA	PU-70K	Flash Memory Address 7
58	FL_ADDR08	I/O	8 mA	PU-70K	Flash Memory Address 8
59	FL_ADDR09	I/O	8 mA	PU-70K	Flash Memory Address 9
61	FL_ADDR10	I/O	8 mA	PU-70K	Flash Memory Address 10
62	FL_ADDR11	I/O	8 mA	PU-70K	Flash Memory Address 11
63	FL_ADDR12	I/O	8 mA	PU-70K	Flash Memory Address 12
64	FL_ADDR13	I/O	8 mA	PU-70K	Flash Memory Address 13
65	FL_ADDR14	I/O	8 mA	PU-70K	Flash Memory Address 14
68	FL_ADDR15	I/O	8 mA	PU-70K	Flash Memory Address 15
69	FL_ADDR16	I/O	8 mA	PU-70K	Flash Memory Address 16
70	FL_ADDR17	I/O	8 mA	PU-70K	Flash Memory Address 17

Table 3-1 SiI3132 Pin Listing

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
71	FL_ADDR18	I/O	8 mA	PU-70K	Flash Memory Address 18
72	FL_RD_N	I/O	8 mA	PU-70K	Flash Memory Read Strobe
73	FL_WR_N	I/O	8 mA	PU-70K	Flash Memory Write Strobe
74	FL_CS_N	I/O	8 mA	PU-70K	Flash Memory Chip Select
76	TMS	I		PU-70K	JTAG Test Mode Select
77	TCK	I-Schmitt			JTAG Test Clock
78	TDI	I		PU-70K	JTAG Test Data In
79	TDO	O	4 mA		JTAG Test Data Out
80	TRSTN	I		PU-70K	JTAG Test Reset
81	SCAN_MODE	I		PD-60K	Internal Scan Mode Control
82	I2C_SDAT	I/O-Schmitt	4 mA	PU-70K	I^2C Serial Data
83	I2C_SCLK	I/O-Schmitt	4 mA	PU-70K	I^2C Serial Clock
86	XTALO	Analog			Crystal Output
87	XTALI/CLKI	Analog			Crystal or Clock Input

Table 3-2 Pin Types	
Pin Type	**Pin Description**
I	Input Pin with LVTTL Thresholds
I-Schmitt	Input Pin with Schmitt Trigger
O	Output Pin
I/O	Bi-directional Pin
I/O-Schmitt	Bi-directional Pin with Schmitt Trigger
OD	Open Drain Output Pin

3.2 Sil3132 Pin Diagram

The diagram below shows the pin layout for the Sil3132.

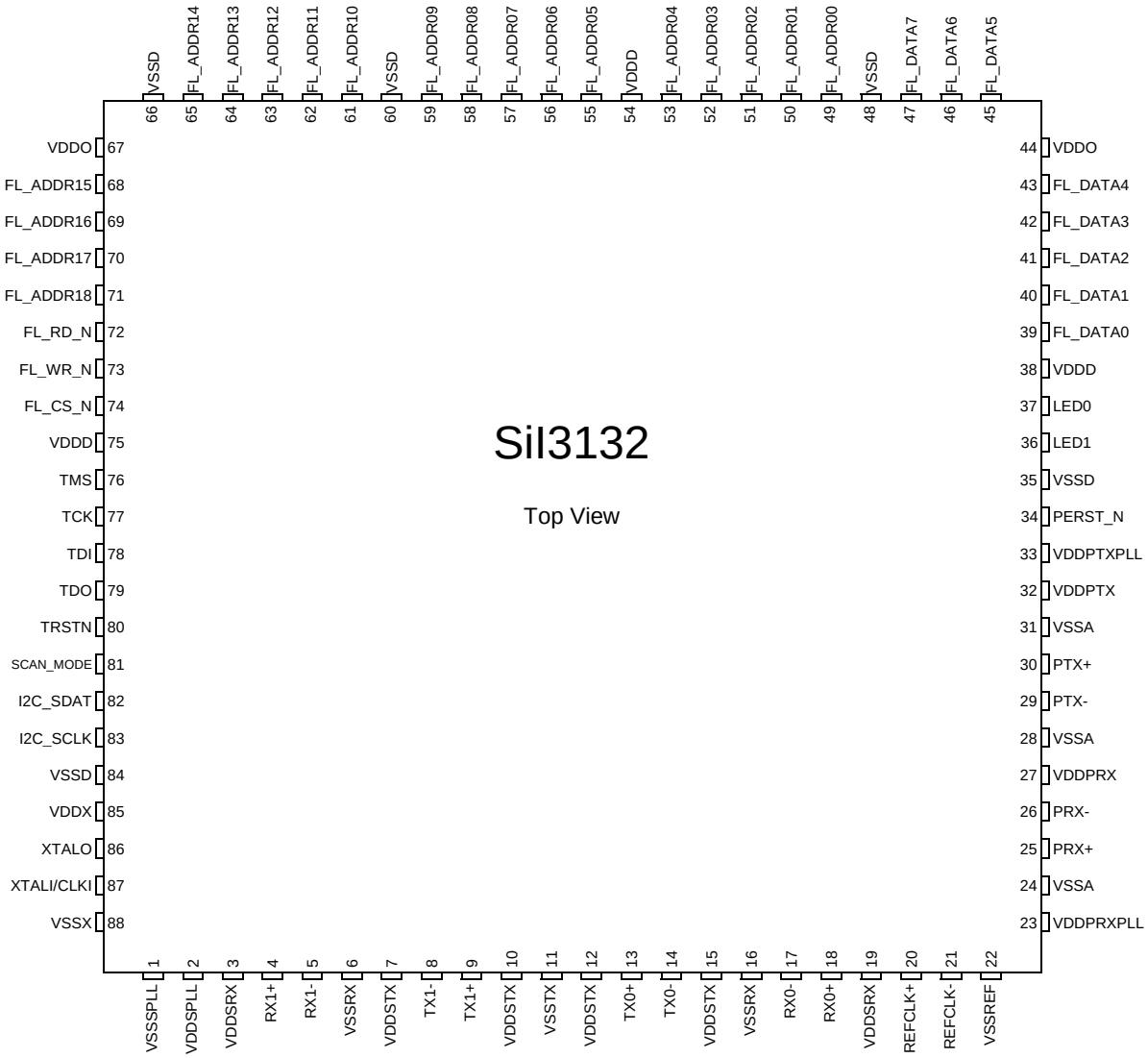


Figure 3-1 Pin Diagram

3.3 Sil3132 Pin Descriptions

3.3.1 PCI Express Pins

Signal Name	Pin Number(s)	Description
PRx+	25	**Receive +.** Serial receiver differential signal, positive side. Must be AC coupled
PRx-	26	**Receive -.** Serial receiver differential signal, negative side. Must be AC coupled
PTx+	30	**Transmit +.** Serial transmitter differential signal, positive side. Must be AC coupled with a 100nF capacitor
PTx-	29	**Transmit -.** Serial transmitter differential signal, negative side. Must be AC coupled with a 100nF capacitor
REFCLK+	20	**Reference Clock +.** PCI Express system supplied differential reference clock, positive side. This input signal must be compliant with PCI Express Card Electromechnical Specification Revision 1.0a
REFCLK-	21	**Reference Clock -.** PCI Express system supplied differential reference clock, negative side. This input signal must be compliant with PCI Express Card Electromechnical Specification Revision 1.0a
PERST_N	34	**Reset.** PERST_N initializes the PCI Express interface and sets internal registers to their initial state.

3.3.2 Flash / I^2C / LED pins

Signal Name	Pin Number(s)	Description
FL_ADDR[18:00]	49-53, 55-59, 61-65, 68-71	**Flash Address.** FL_ADDR[18:00] is the Flash Memory address for up to 512K of Flash Memory.
FL_DATA[07:00]	39-43, 45-47	**Flash Data.** 8-bit Flash memory data bus
FL_RD_N	72	**Flash Read Enable.** Active low
FL_WR_N	73	**Flash Write Enable.** Active low
FL_CS_N	74	**Flash Chip Select.** Active low
I2C_SDAT	82	**I^2C Serial Data.** Serial Interface (I^2C) data line (internally connected to PHY I^2C data line)
I2C_SCLK	83	**I^2C Serial Clock.** Serial Interface (I^2C) clock (internally connected to PHY I^2C clock)
LED[1:0]	36, 37	**Activity LED.** Activity LED drivers for channels 1 and 0.

3.3.3 Serial ATA Signals

Signal Name	Pin Number(s)	Description
Rx[1:0]+	4, 18	**Receive +.** Serial receiver differential signal, positive side. Must be AC coupled
Rx[1:0]-	5, 17	**Receive -.** Serial receiver differential signal, negative side. Must be AC coupled
Tx[1:0]+	9, 13	**Transmit +.** Serial transmitter differential signal, positive side. Must be AC coupled
Tx[1:0]-	8, 14	**Transmit -.** Serial transmitter differential signal, negative side. Must be AC coupled
XTALI/CLKI	87	**Crystal In.** Crystal oscillator pin for SerDes reference clock. When external clock source is selected, the 25MHz external clock will come in through this pin. The clock must be 1.8V swing and the precision recommendation is ±50ppm. Please refer Table 2-10 CLKI SerDes Reference Clock Input Requirements for the detail
XTALO	86	**Crystal Out.** Crystal oscillator pin for SerDes reference clock. A 25MHz crystal must be used.

3.3.4 Test Pins

Signal Name	Pin Number(s)	Description
TMS	76	**JTAG Test Mode Select**
TCK	77	**JTAG Test Clock**
TDI	78	**JTAG Test Data In**
TDO	79	**JTAG Test Data Out**
TRSTN	80	**JTAG Test Reset. This pin must be tied to ground if JTAG function is not used.**
SCAN_MODE	81	**Scan Mode. Used for factory testing; do not connect.**

3.3.5 Power/Ground Pins

All like-named power/ground pins, in the table below, are connected together within the package.

Pin Name	Pin Number(s)	Description
VDDSRX	3, 19	**Receiver Power.** These pins provide 1.8V for the Serial ATA receivers.
VSSRX	6, 16	**Receiver Ground.** These pins provide the Ground reference for the Serial ATA receivers.
VDDSTX	7, 10, 12, 15	**Transmitter Power.** These pins provide 1.8V for the Serial ATA transmitters.
VSSTX	11	**Transmitter Ground.** This pin provides the Ground reference for the Serial ATA transmitters.
VDDPRX	27	**Receiver Power.** This pin provides 1.8V for the PCI Express receivers.
VDDPTX	32	**Transmitter Power.** This pin provides 1.8V for the PCI Express transmitters.
VDDPTXPLL	33	**PLL Power.** This pin provides 1.8V for the PCI Express transmitter PLL.
VDDPRXPLL	23	**PLL Power.** This pin provides 1.8V for the PCI Express receiver PLL.
VSSA	24, 28, 31	**PCI-E Ground.** These pins provide the Ground reference for the PCI Express SerDes.
VDDSPLL	2	**PLL Power.** This pin provides 1.8V for the Serial ATA PLL and crystal oscillator.
VSSSPLL	1	**PLL Ground.** This pin provides the Ground reference for the Serial ATA PLL.
VSSREF	22	**Reference Clock Ground.** This pin provides the Ground reference for the PCI-Express reference clock receiver.
VDDX	85	**Oscillator Power.** This pin provides 1.8V for the crystal oscillator (associated with XTALI and XTALO pins).
VSSX	88	**Oscillator Ground.** This pin provides the Ground reference for the crystal oscillator (associated with XTALI and XTALO pins).
VDDO	44, 67	**I/O Power.** These pins provide 3.3V for the digital I/O.
VDDD	38, 54, 75	**Digital Power.** These pins provide 1.8V for the digital logic.
VSSD	35, 48, 60, 66, 84	**Digital Ground.** These pins provide the Ground reference for the digital portion of the chip.

4 Package Drawing

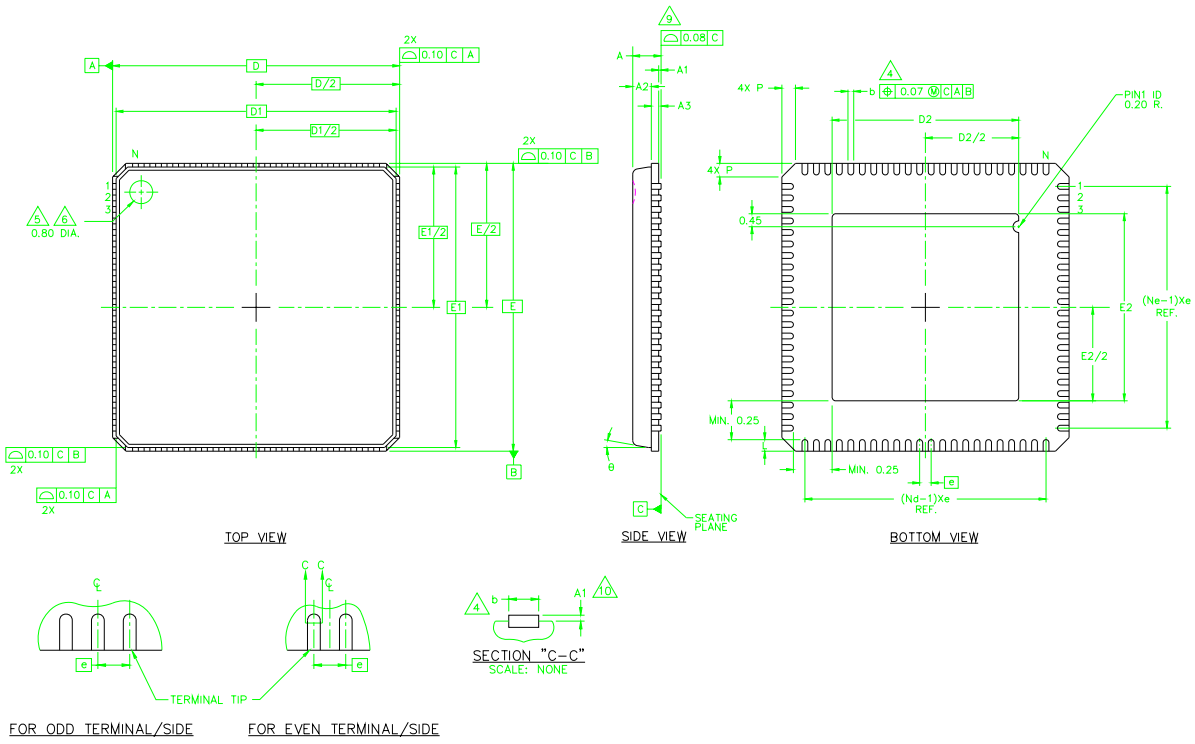


Figure 4-1 Package Drawing 88 QFN

Symbol	Dimensions (mm)		
	Minimum	Nominal	Maximum
e		0.40	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D2	5.85	6.00[1]	6.65
E2	5.85	6.00[1]	6.65
A	-	0.85	0.90
A1	0.00	0.02	0.05
A2	-	0.65	0.70
A3	0.20 REF		
D	10.00 BSC		
D1	9.75 BSC		
E	10.00 BSC		
E1	9.75 BSC		
θ			12°
P	0.24	0.42	0.60

Table 4-1 Package Dimensions

Note: [1] **It is required that an EPAD is soldered to PCB ground** and the landing area be incorporated on the PCB within the footprint of the package corresponding to the EPAD. The size of this landing area can be larger than the exposed pad on the package, **should be at least the same as the maximum size of exposed pad of the package (6.65 x 6.65mm). If the traces are within the maximum size of exposed pad, the trace may short to the exposed pad when the package has the exposed pad with the maximum dimension.**

Part Ordering Number:

SiI3132CNU (88 pin QFN lead free package with an exposed pad)

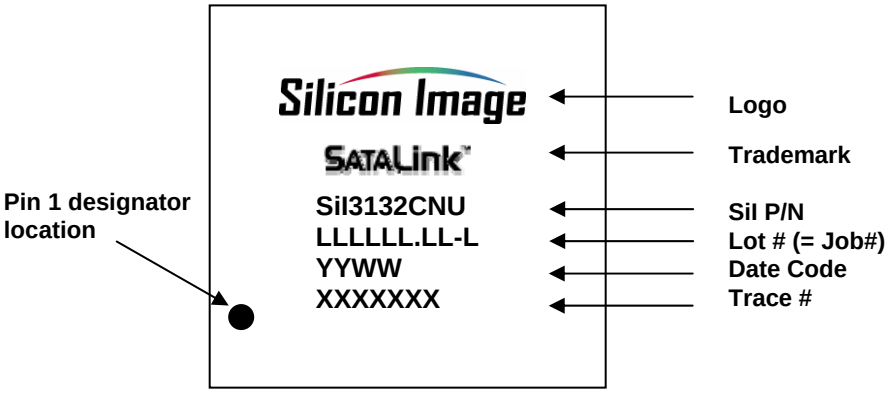


Figure 4-2 Marking Specification

5 Programming Model

5.1 Sil3132 Block Diagram

The Sil3132 contains the major logic modules shown below.

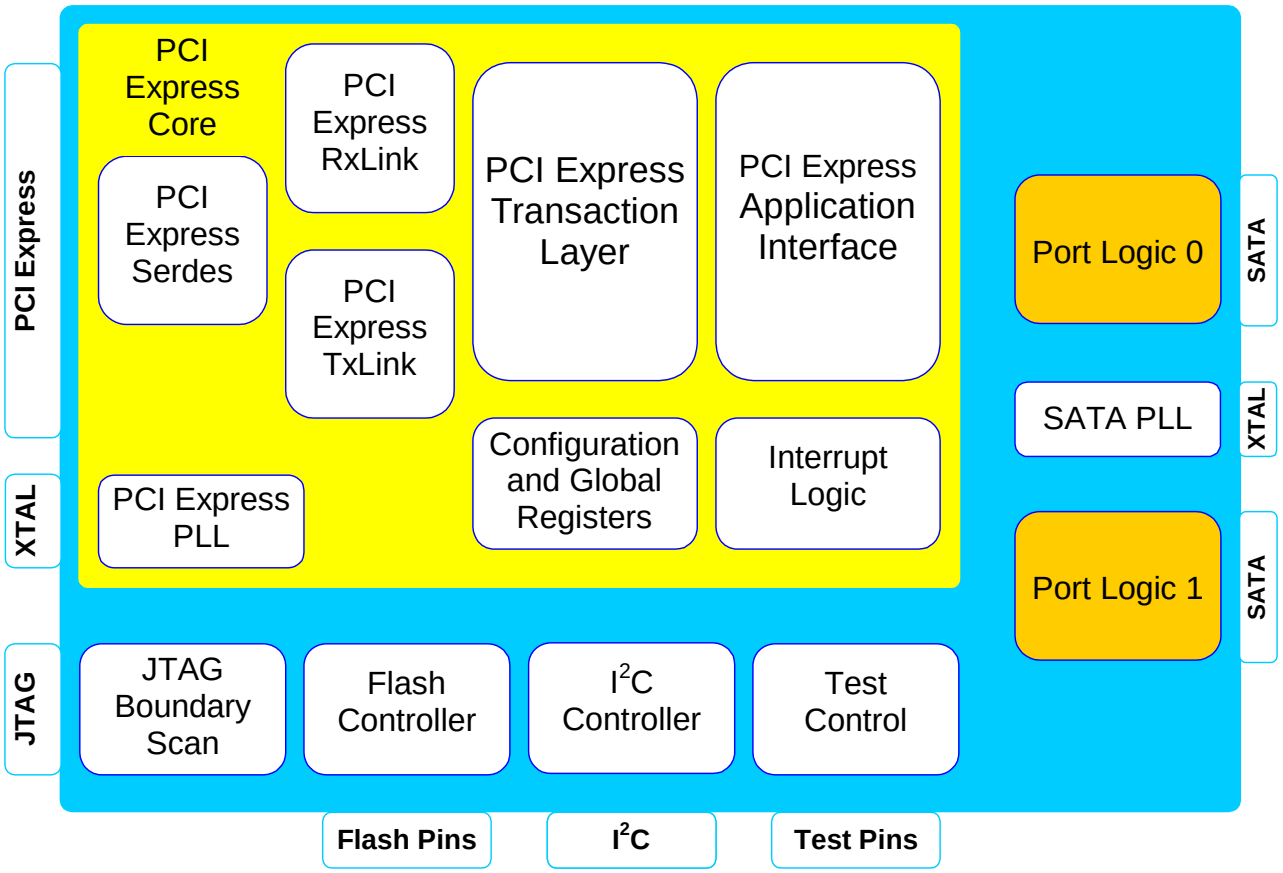


Figure 5-1 Sil3132 Block Diagram

The PCI Express Core logic block provides PCI Express 1.0a compatibility. The Global Register File block corresponds to the registers addressed by Base Address Register 0.

The initialization function provided by the I^2C Controller and Flash Controller is described in Section 6, Auto-Initialization, on page 21.

6 Auto-Initialization

The SiI3132 supports an external Flash and/or EEPROM device for BIOS extensions and user-defined PCI configuration header data.

6.1 Auto-Initialization from Flash

The SiI3132 initiates the Flash detection and configuration space loading sequence upon the release of PERST#. It begins by reading the highest two addresses ($7FFFF_H$ and $7FFFE_H$), checking for the correct data signature pattern – AA_H and 55_H, respectively. If the data signature pattern is correct, the SiI3132 continues to sequence the address downward, reading a total of twelve bytes. If the Data Signature is correct (55_H at $7FFFC_H$), the last eight bytes are loaded into the PCI Configuration Space registers.

If both Flash and EEPROM are installed, the PCI Configuration Space registers will be loaded with the EEPROM's data.

While the sequence is active, the SiI3132 responds to all PCI bus accesses with a Target Retry.

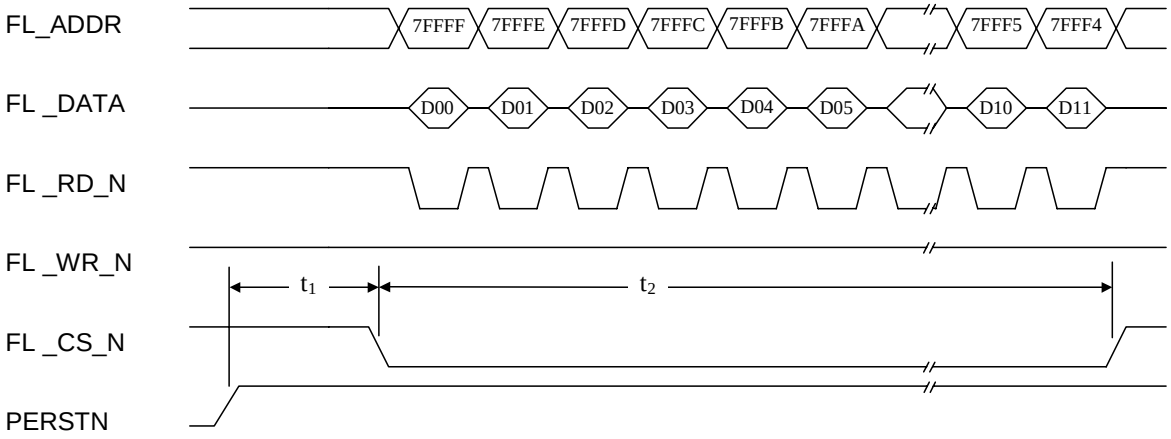


Figure 6-1 Auto-Initialization from Flash Timing

Parameter	Value	Description
t_1	660 ns	PCI reset to Flash Auto-Initialization cycle begin
t_2	4200 ns	Flash Auto-Initialization cycle time

Table 6-1 Auto-Initialization from Flash Timing

Address	Data Byte	Description
$7FFFF_H$	D00	Data Signature = AA_H
$7FFFE_H$	D01	Data Signature = 55_H
$7FFFD_H$	D02	AA = 120 ns Flash device / Else, 240 ns Flash device
$7FFFC_H$	D03	Data Signature = 55_H
$7FFFB_H$	D04	PCI Device ID [23:16]
$7FFFA_H$	D05	PCI Device ID [31:24]
$7FFF9_H$	D06	PCI Class Code [15:08]
$7FFF8_H$	D07	PCI Class Code [23:16]
$7FFF7_H$	D08	PCI Sub-System Vendor ID [07:00]
$7FFF6_H$	D09	PCI Sub-System Vendor ID [15:08]
$7FFF5_H$	D10	PCI Sub-System ID [23:16]
$7FFF4_H$	D11	PCI Sub-System ID [31:24]

Table 6-2 Flash Data Description

6.2 Auto-Initialization from EEPROM

The SiI3132 initiates the EEPROM detection and configuration space loading sequence after the Flash read sequence. The SiI3132 supports EEPROMs with an I^2C serial interface. The sequence of operations consists of the following.

1) START condition defined as a high-to-low transition on I2C_SDAT while I2C_SCLK is high.
2) Control byte = 1010 (Control Code) + 000 (Chip Select) + 0 (Write Address)
3) Acknowledge
4) Starting address field = 00000000.
5) Acknowledge
6) Sequential data bytes separated by Acknowledges.
7) STOP condition.

While the sequence is active, the SiI3132 responds to all PCI bus accesses with a Target Retry.

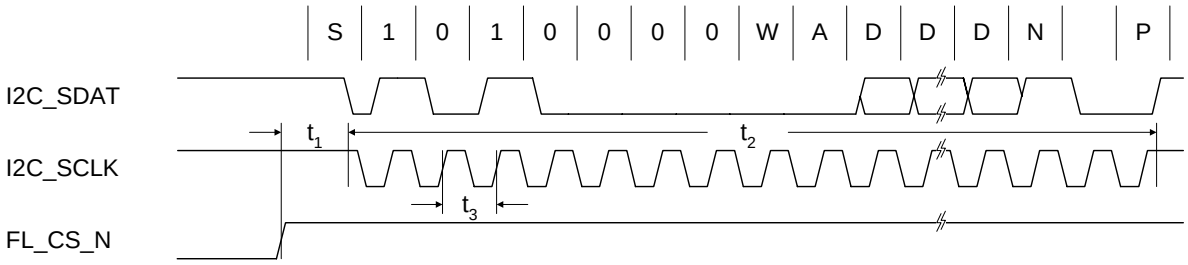


Figure 6-2 Auto-Initialization from EEPROM Timing

Parameter	Value	Description
t_1	26.00 µs	End of Auto-Initialization from Flash to start of Auto-Initialization from EEPROM
t_2	1.4 ms	Auto-Initialization from EEPROM cycle time
t_3	10 µs	EEPROM serial clock period

Table 6-3 Auto-Initialization from EEPROM Timing

Parameter	Description
S	START condition
W	R/W 0 = Write Command, 1 = Read Command
A	Acknowledge
D	Serial data
N	No-Acknowledge
P	STOP condition

Table 6-4 Auto-Initialization from EEPROM Timing Symbols

Address	Data Byte	Description
00_H	D00	Memory Present Pattern = AA_H
01_H	D01	Memory Present Pattern = 55_H
02_H	D02	Data Signature = AA_H
03_H	D03	Data Signature = 55_H
04_H	D04	PCI Device ID [23:16]
05_H	D05	PCI Device ID [31:24]
06_H	D06	PCI Class Code [15:08]
07_H	D07	PCI Class Code [23:16]
08_H	D08	PCI Sub-System Vendor ID [07:00]
09_H	D09	PCI Sub-System Vendor ID [15:08]
$0A_H$	D10	PCI Sub-System ID [23:16]
$0B_H$	D11	PCI Sub-System ID [31:24]

Table 6-5 EEPROM Data Description

7 Power Management

The following register bits control Power Management in a SiI3132 Port.

Register	Bits	Description
Interrupt Status	PM Change Bit 3	This bit reports a change in the Power Management mode. It corresponds to the interrupt enabled by bit 3 of the Port Interrupt Enable register.
SError	W Bit 18	This bit reports a ComWake received from the Serial ATA bus. It corresponds to the interrupt enabled by bit 5 of the Port Interrupt Enable register.
Interrupt Status	ComWake Bit 5	
SControl	SPM Bits 15-12	This bit field initiates transitions to/from Partial or Slumber power management states; bit 14 corresponds to ComWake (exit power management); bit 13 corresponds to Slumber mode; bit 12 corresponds to Partial mode.
SControl	IPM Bits 11-8	This bit field disables transitions to Partial or Slumber power management states; bit 9 corresponds to Slumber mode; bit 8 corresponds to Partial mode.
SStatus	IPM Bits 11-8	This bit field reports the power management state; '0110' corresponds to Slumber mode; '0010' corresponds to Partial mode.

Table 7-1 Power Management Register Bits

There are two power management modes: Partial and Slumber. These power management modes may be software initiated through the SControl register or device initiated from the Serial ATA device.

Transitions to and from either power management mode generate an interrupt, the Power Management Mode Change Interrupt, which may be masked in the Port Interrupt Enable register (bit 3).

Partial/Slumber mode may be initiated by software through the SControl register. By setting the SPM field to either '0001' (Partial) or '0010' (Slumber), software causes a PMREQ to the Serial ATA device, which will respond with either a PMACK or PMNAK. If a PMACK is received the Partial/Slumber mode is entered. A PMNAK is ignored; the request remains asserted.

The Serial ATA device may initiate Partial/Slumber mode. Software enables the acknowledgement of this request by setting the IPM field in the SControl register to '0001' (Partial), '0010' (Slumber), or '0011' (Partial or Slumber). If enabled, a PMACK will be sent to the device; if not enabled, a PMNAK will be sent. When the request is received and its acknowledgement is enabled, Partial/Slumber mode is entered.

Partial/Slumber mode status is reported in the SStatus register ('0010'/'0110' in the IPM field).

Partial/Slumber mode is cleared by ComWake (asserted when the SPM field is set to '0100').

8 Flash, GPIO, EEPROM, and I²C Programming

8.1 Flash Memory Access

The SiI3132 supports an external Flash memory device of up to 4 Mbits (512 KBytes) in capacity. Access to the Flash memory is available using either PCI Direct Access or Register Access.

8.1.1 PCI Direct Access

Access to the Expansion Rom is enabled by setting bit 0 in the Expansion Rom Base Address register at Offset 30h of the PCI Configuration Space. When this bit is set, bits [31:19] of the same register are programmable by the system to set the base address for all Flash memory accesses. Read and write operations with the Flash memory are initiated by Memory Read and Memory Write commands on the PCI bus. Accesses may be as Bytes, Words, or DWords.

8.1.2 Register Access

This type of Flash memory access is carried out through a sequence of internal register read and write operations. The proper programming sequences are detailed below.

8.1.2.1 Flash Write Operation

Verify that Flash Address register bit 25 (Mem Access Start) is zero. The bit is one when a memory access is in progress. It is zero when the memory access is complete and ready for another operation.

Program the write address for the Flash memory access. The address field is bits [18:0] in the Flash Address register.

Program the write data for the Flash memory access. The data field is bits [7:0] in the Flash Memory Data register.

Program Flash Address register bit 24 (Mem Access Type) to zero for a memory write.

Initiate the Flash memory access by setting bit 25 in the Flash Address register.

8.1.2.2 Flash Read Operation

Verify that Flash Address register bit 25 (Mem Access Start) is zero. The bit is one when a memory access is in progress. It is zero when the memory access is complete and ready for another operation.

Program the read address for the Flash memory access. The address field is bits [18:0] in the Flash Address register.

Program Flash Address register bit 24 (Mem Access Type) to one for a memory read.

Initiate the Flash memory access by setting bit 25 in the Flash Address register.

Verify that Flash Address register bit 25 (Mem Access Start) is clear. The bit is one when a memory access is in progress. It is zero when the memory access is complete.

Read the data from bits [7:0] in the Flash Memory Data register.

8.2 I²C Operation

The SiI3132 provides a Multimaster I²C interface. For Auto-initialization of some PCI Configuration registers an external 256-byte EEPROM memory device may be connected to this I²C interface (see section 6). Two registers are provided for programmed read/write access to the I²C interface: the I²C Address register and the I²C Data/Control register.

8.2.1.1 I²C Write Operation

Verify that I²C Data/Control register bit 31 (I²C Access Start) is zero. The bit is one when an access is in progress. It is zero when the access is complete and another operation may be started.

Write '1' to clear bit 28 in the I²C Data/Control register. This bit is set if an error occurred during a previous access.

Program the write address for the access in the I²C Address register.

Program the write data for the access in the I²C Data/Control register (bits 7:0).

Write zero to bit 24 (I²C Access Type) in the I²C Address register.

Initiate the I²C write by setting bit 31 (I²C Access Start) in the I²C Data/Control register.

Poll bit 31 in the I²C Data/Control register. The bit is one while an access is in progress. It becomes zero when the access completes. (Alternatively, the I²C Interrupt may be enabled by the Global Control register and Global Interrupt Status register)

Check bit 28 in the I²C Data/Control register. The bit is set if an error occurred during the access.

8.2.1.2 I²C Read Operation

Verify that I²C Data/Control register bit 31 (I²C Access Start) is zero. The bit is one when an access is in progress. It is zero when the access is complete and another operation may be started.

Write '1' to clear bit 28 in the I²C Data/Control register. The bit is set if an error occurred during a previous access.

Program the read address for the access in the I²C Address register.

Write one to bit 24 (I²C Access Type) in the I²C Address register.

Initiate the I²C read by setting bit 31 (I²C Access Start) in the I²C Data/Control register.

Poll bit 31 in the I²C Data/Control register. The bit is one while an access is in progress. It becomes zero when the access completes. (Alternatively, the I²C Interrupt may be enabled by the Global Control register and Global Interrupt Status register.)

Check bit 28 in the I²C Data/Control register. The bit is set if an error occurred during the access.

Read the data from bits 7:0 in the I²C Data/Control register.

Legal Statement

Copyright Notice

Trademark Acknowledgment

Disclaimers

Further Information
To request other materials, documentation, and information, contact your local Silicon Image, Inc. sales office or visit the Silicon Image, Inc. web site at www.siliconimage.com.