

Sil3512 Production Board

- Reference schematics -

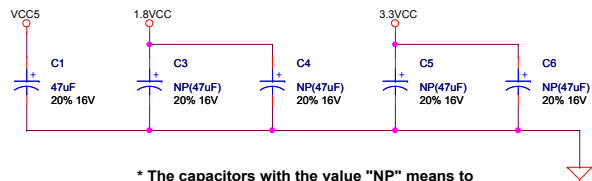
NOTES: Unless Otherwise Specified:

1. All components are subject to change.
2. All resistors and ceramic capacitors are in surface mount 0603 package unless otherwise specified
3. All resistors are 5%, 1/16 watt unless otherwise specified
4. All capacitors are 20%, 50 volt ceramic unless otherwise specified
5. Only location U3 or location Y1 can be populated at a time. If location U3 is populated, then locations R2,R3,C18,C19 and L3 must be installed and Y1, C62, C63 and R10 must be emptied. Else if, location Y1 is populated, then C62, C63 and R10 must be installed and R3 (U3,R2,R3,C18,C19 and L3) must be emptied. Y1 is installed by default.
6. R9 must be replaced by 4.99K 1% with 100MHz reference clock at XTALI. R9 is 1K 1% by default with 25MHz reference clock.

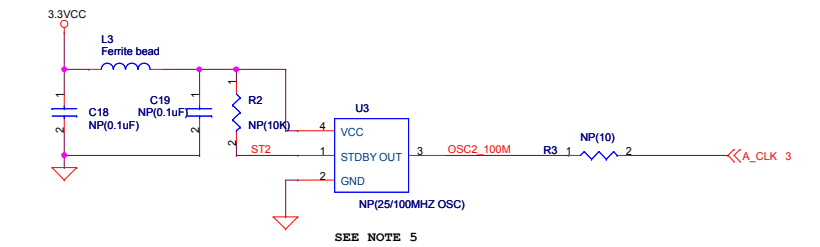
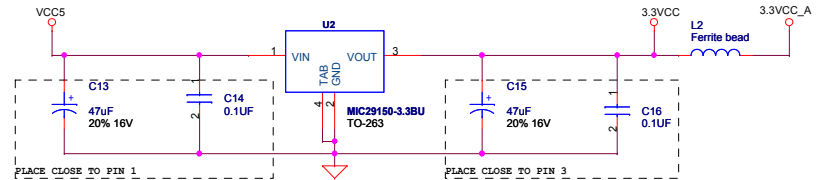
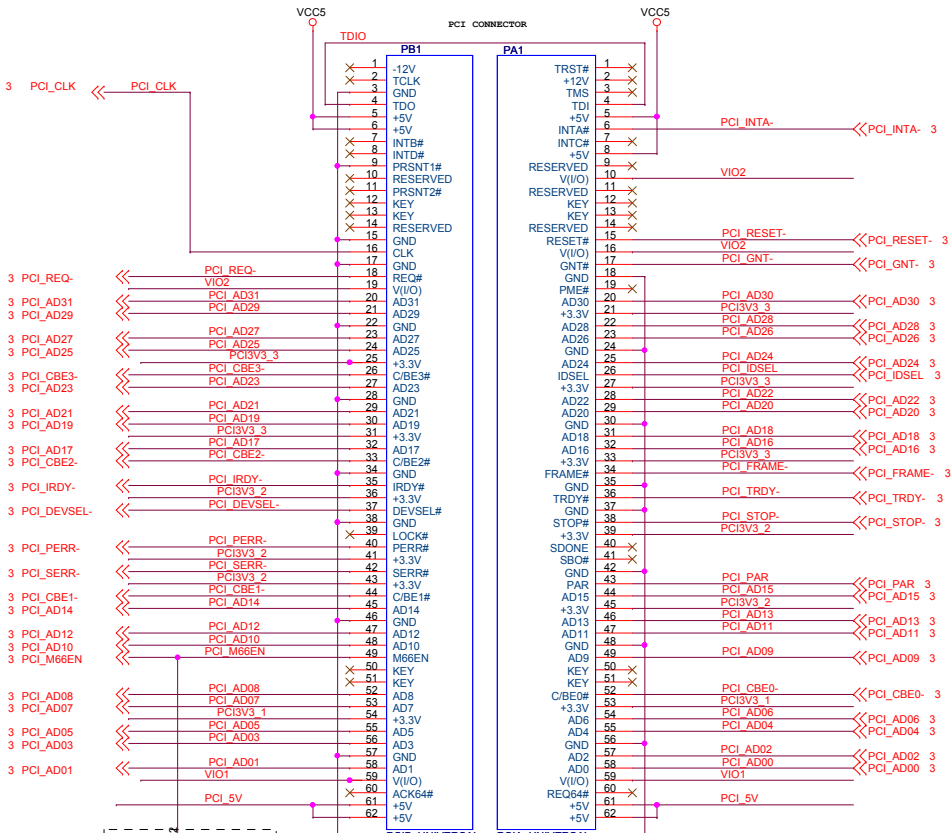
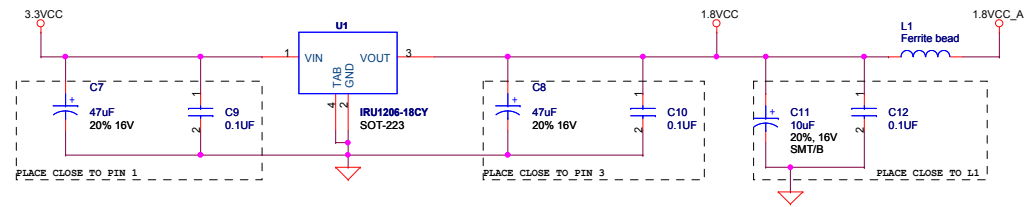
Rev A
- Derived from Preliminary schematics Rev 0.96
- Added comment for that EPAD must be soldered to the PCB GND
Rev.B
- Corrected SATA connectors pin assignments

Reference Schematic ONLY.
Please consult Silicon Image.

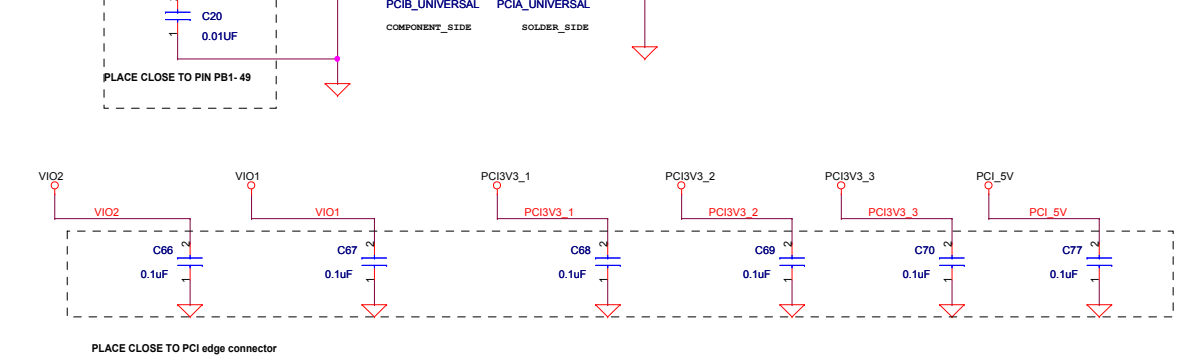
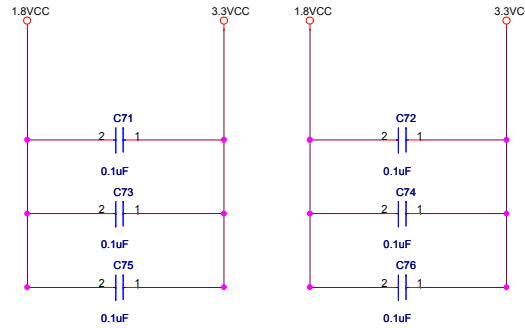
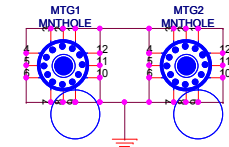
Title			
PB3512 Rev. D			
Size	Document Number	Rev	
Custom	Sil-SC-0056-B	D	
Date:	Monday, August 07, 2006	Sheet	1 of 3



* The capacitors with the value "NP" means to prepare the pad but not installed.

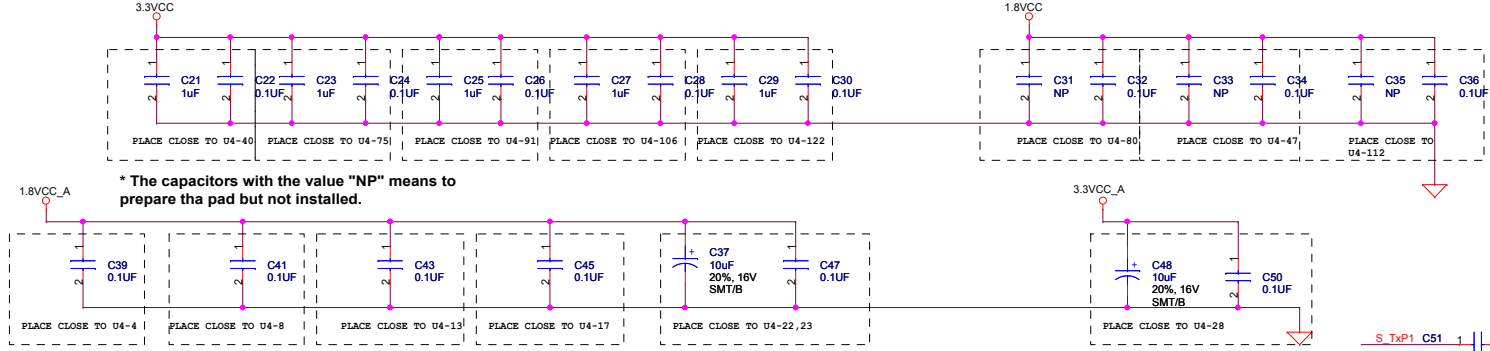


SEE NOTE 5

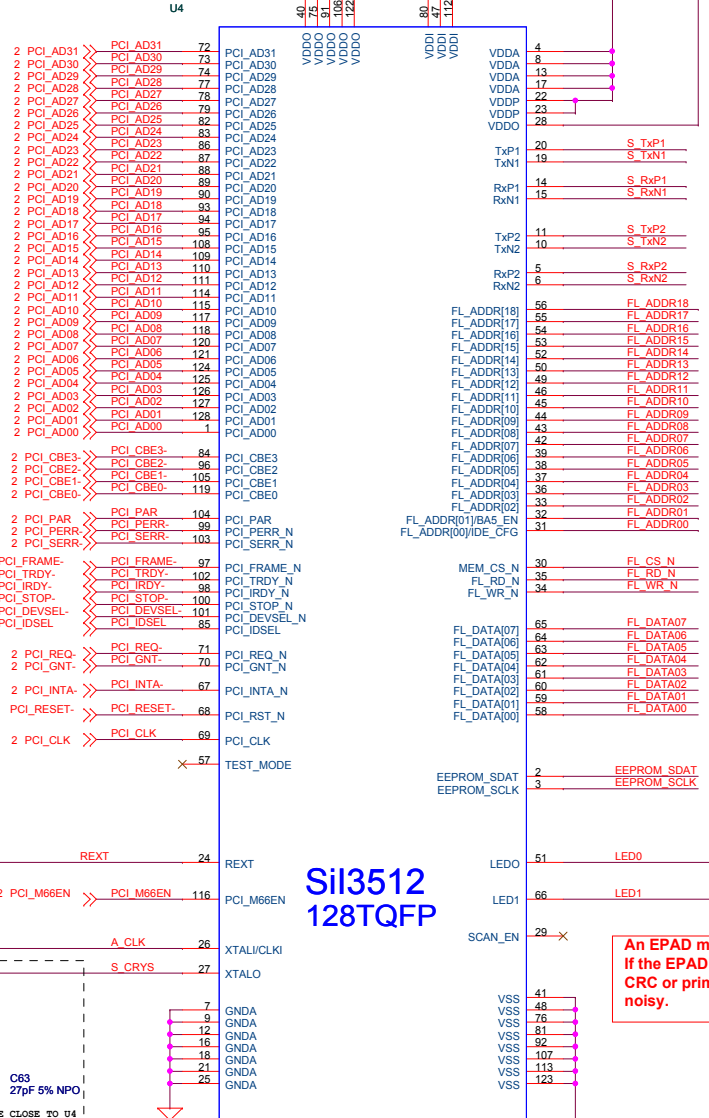
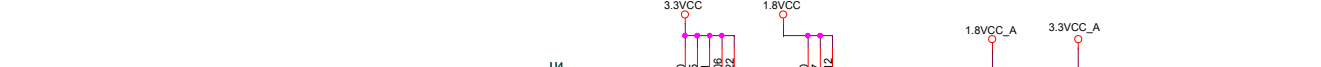


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Title			PB3512 Rev. D		
Size	Document Number				Rev
Custom	SII-SC-0056-B				D
Date:	Monday, August 07, 2006	Sheet	2	of	3

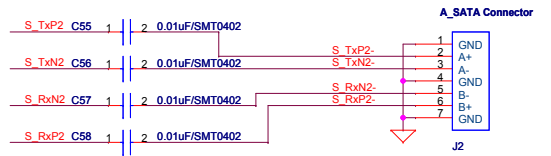
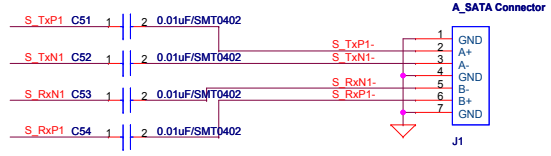


* The capacitors with the value "NP" means to prepare the pad but not installed.

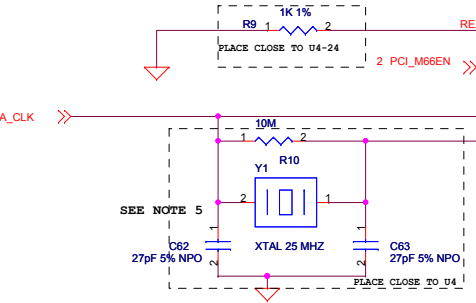
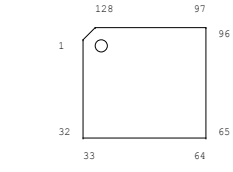
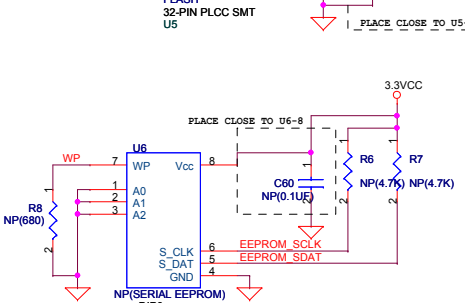
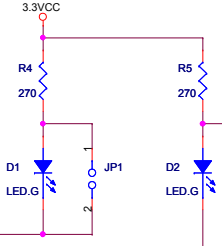
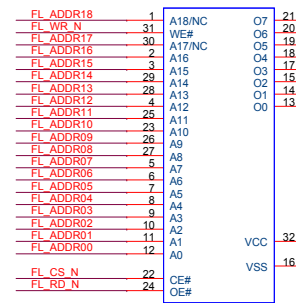


**SiI3512
128TQFP**

An EPAD must be soldered to the PCB GND. If the EPAD is not soldered, it may result in CRC or primitive error if the environments are noisy.



SATA Connectors with gold fingers facing down (standard)



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Title		PB3512 Rev. D	
Size	Document Number	SiI-SC-0056-B	
Custom	Date:	Monday, August 07, 2006	Sheet 3 of 3