

TABLE 1A: JP1 JUMPER SETTING

JP1 Jumper Status	IDE/RAID Mode	Note
IN	RAID MODE	
OUT	IDE MODE	

TABLE 1B: JP2 JUMPER SETTING

JP2 Jumper Status	BA5 ENABLE/DISABLE	Note
IN	DISABLE	
OUT	ENABLE	

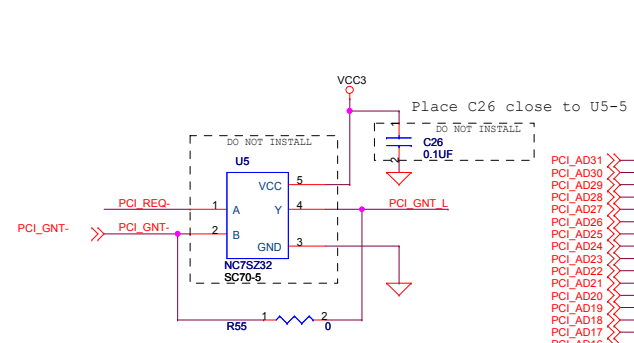
TABLE 2: DEVICES SUPPORTED IN LOCATION U4

MEMORY TYPE	FLASH MEMORY	FLASH MEMORY
FLASH MEMORY MODELS [5V]	AMD AM29F010B 1Mbit [128k x 8]	AMD AM29F040B 4Mbit [512k x 8]
NOTE	DEFAULT	

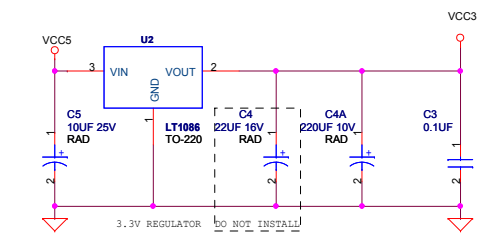
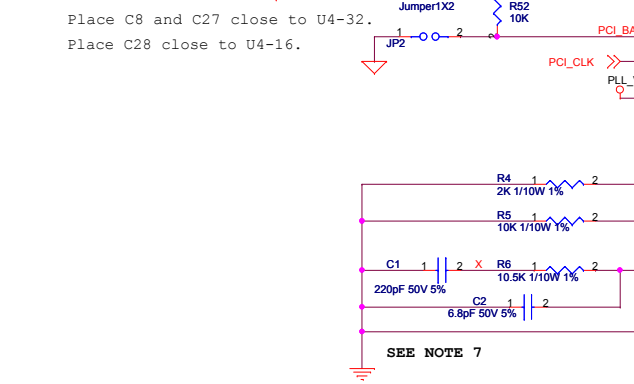
NOTES: Unless Otherwise Specified:

1. All components are subject to change.
2. All resistors and capacitors are in surface mount 0805 package.
3. All resistors are 5%, 1/8 watt.
4. All capacitors are 20%, 50 volt ceramic.
5. The following resistors are 1%, 1/10 watt: R4,R5,R6,R16 and R26.
6. The following capacitors are 5%, 50 Volt, NPO: C1,C2.
7. Circuit board layout and component selection are critical to the proper operation of the PLL. Refer to the PCI-680 Product Specification, PLL Chapter, for the circuit board layout and component selection requirements.
8. If the PCI bus provides 3.3 Volt power, and if it is desired to use this power, then locations R32 and R33 must be populated with zero ohm resistors, and U2 must not be populated. Only one power path (U2 or R32,R33) can be populated at a time.

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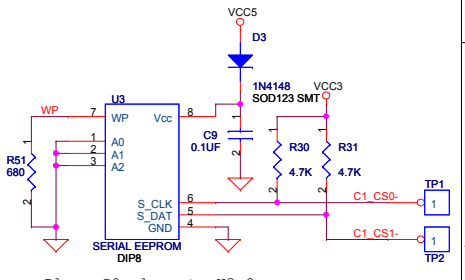
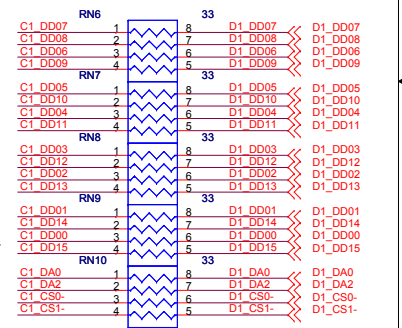
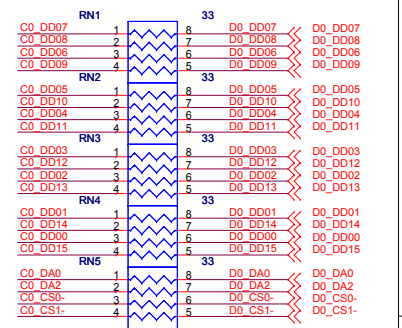
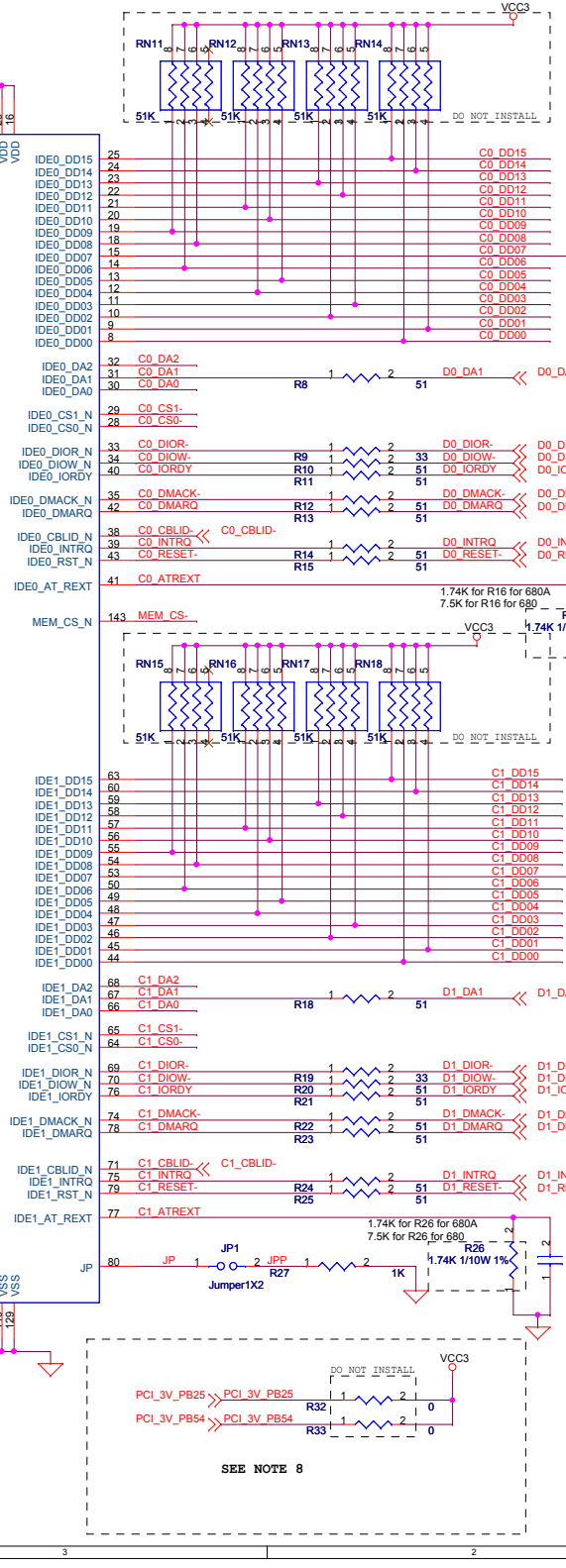
U4	
C0_DD00	1
C0_CS1-	31
C0_DD01	30
C0_DD02	2
C0_DD03	3
C0_DD04	29
C0_DD05	28
C0_DD06	4
C0_DD07	25
C0_DD08	23
C0_DD09	26
C0_DD10	27
C0_DD11	5
C0_DD12	6
C0_DD13	7
C0_DD14	8
C0_DD15	9
C0_DA0	A3
C0_DA1	A1
C0_DA2	A0
MEM_CS-	22
C0_CS0-	24
A18/NC	07
WE#	06
A17/NC	05
A16	04
A15	03
A14	02
A13	01
A12	00
A11	00
A10	00
A9	00
A8	00
A7	00
A6	00
A5	00
A4	00
A3	00
A1	00
A0	00
CE#	00
OE#	00



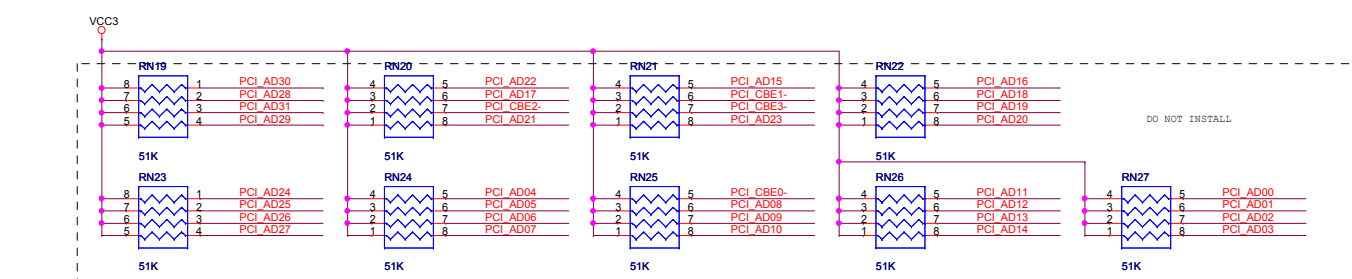
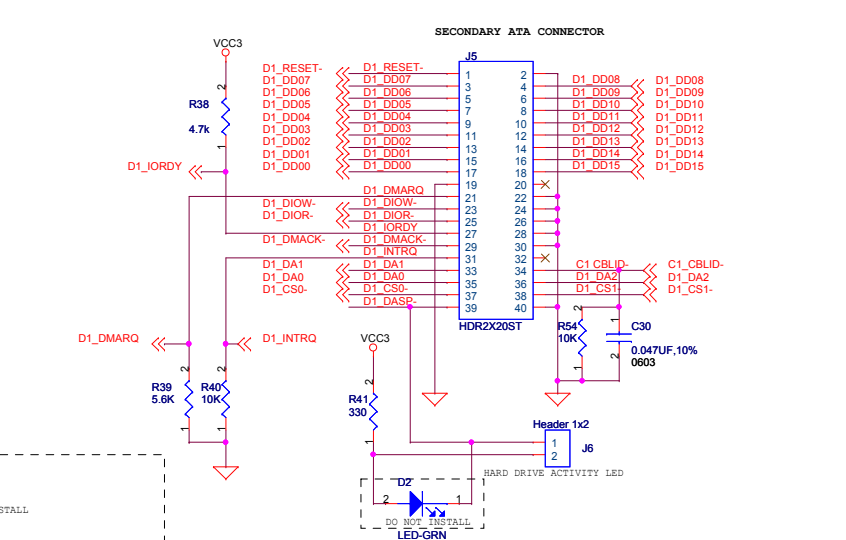
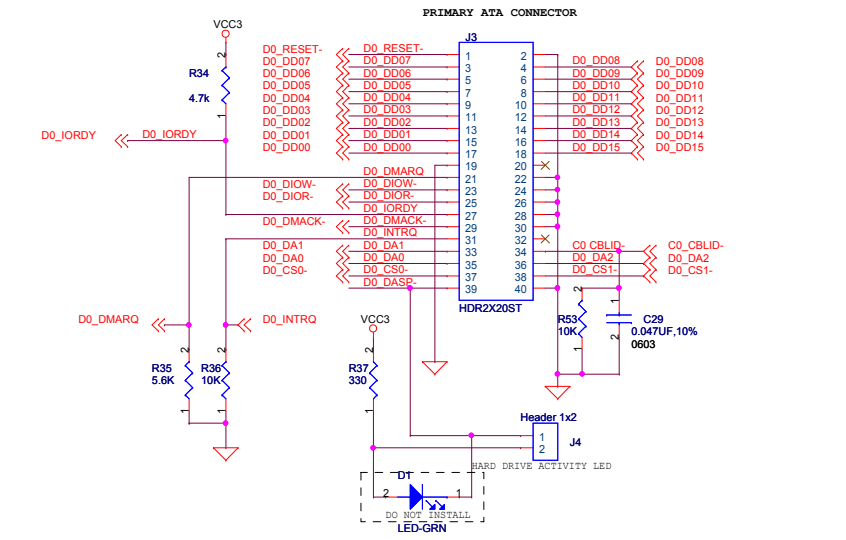
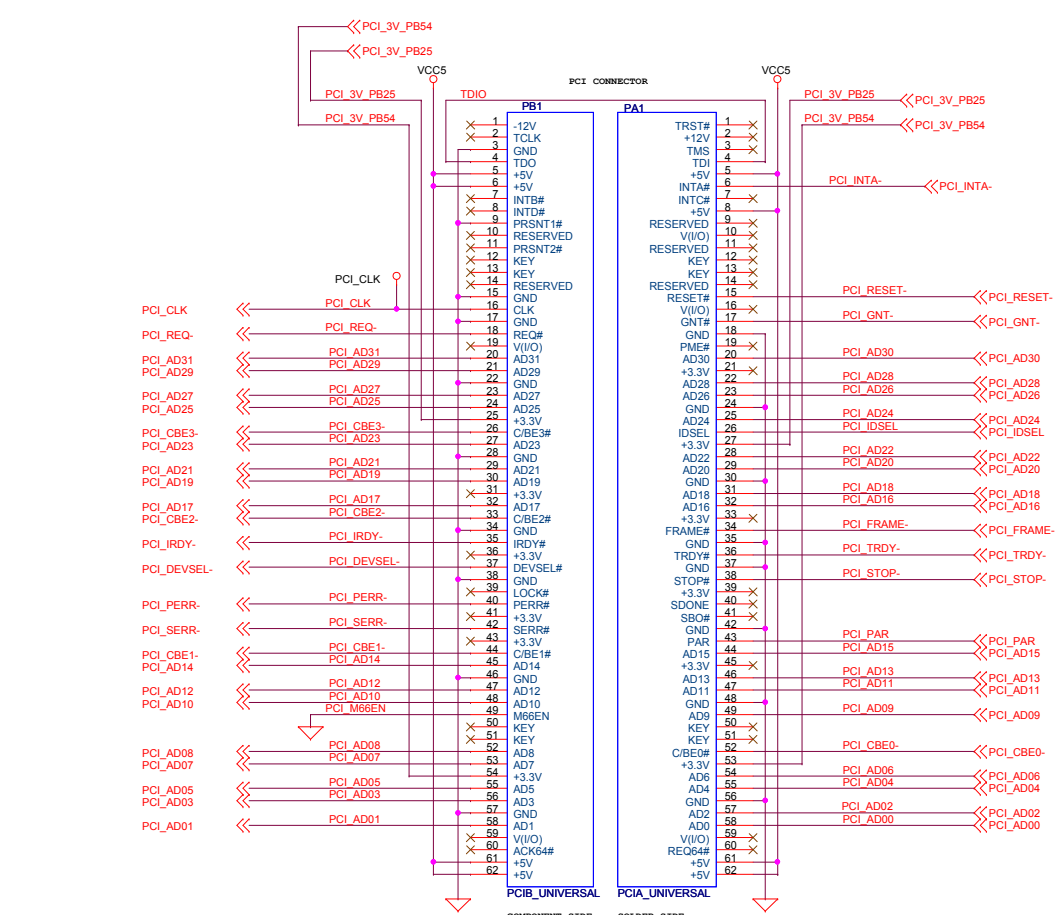
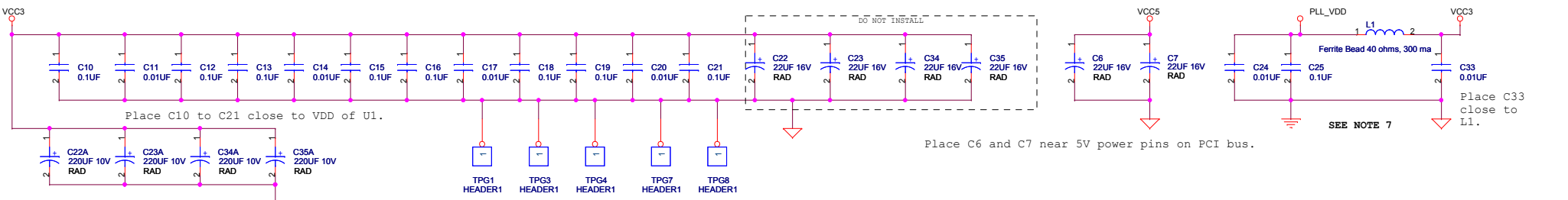
PCI_AD31	81	PCI_AD31	81
PCI_AD30	82	PCI_AD30	82
PCI_AD29	83	PCI_AD29	83
PCI_AD28	84	PCI_AD28	84
PCI_AD27	85	PCI_AD27	85
PCI_AD26	86	PCI_AD26	86
PCI_AD25	87	PCI_AD25	87
PCI_AD24	88	PCI_AD24	88
PCI_AD23	89	PCI_AD23	89
PCI_AD22	90	PCI_AD22	90
PCI_AD21	91	PCI_AD21	91
PCI_AD20	92	PCI_AD20	92
PCI_AD19	93	PCI_AD19	93
PCI_AD18	94	PCI_AD18	94
PCI_AD17	95	PCI_AD17	95
PCI_AD16	96	PCI_AD16	96
PCI_AD15	97	PCI_AD15	97
PCI_AD14	98	PCI_AD14	98
PCI_AD13	99	PCI_AD13	99
PCI_AD12	100	PCI_AD12	100
PCI_AD11	101	PCI_AD11	101
PCI_AD10	102	PCI_AD10	102
PCI_AD09	103	PCI_AD09	103
PCI_AD08	104	PCI_AD08	104
PCI_AD07	105	PCI_AD07	105
PCI_AD06	106	PCI_AD06	106
PCI_AD05	107	PCI_AD05	107
PCI_AD04	108	PCI_AD04	108
PCI_AD03	109	PCI_AD03	109
PCI_AD02	110	PCI_AD02	110
PCI_AD01	111	PCI_AD01	111
PCI_AD00	112	PCI_AD00	112

PCI_CBE3-	91	PCI_CBE3-	91
PCI_CBE2-	103	PCI_CBE2-	103
PCI_CBE1-	114	PCI_CBE1-	114
PCI_CBE0-	126	PCI_CBE0-	126
PCI_PAR	113	PCI_PAR	113
PCI_PERR-	111	PCI_PERR-	111
PCI_SERR-	112	PCI_SERR-	112
PCI_FRAME-	104	PCI_FRAME-	104
PCI_TRDY-	106	PCI_TRDY-	106
PCI_IRDY-	105	PCI_IRDY-	105
PCI_STOP-	110	PCI_STOP-	110
PCI_DEVSEL-	107	PCI_DEVSEL-	107
PCI_IDSEL	124	PCI_IDSEL	124
PCI_REQ-	136	PCI_REQ-	136
PCI_GNT_L	137	PCI_GNT_L	137
PCI_INTA-	138	PCI_INTA-	138
PCI_RESET-	141	PCI_RESET-	141
PCI_BAS_EN	139	PCI_BAS_EN	139
PCI_CLK	140	PCI_CLK	140
PLL_VDD	2	PLL_VDD	2
PLL_CPBIAS	3	PLL_CPBIAS	3
PLL_VCOBIAS	4	PLL_VCOBIAS	4
PLL_LOOPFLT	5	PLL_LOOPFLT	5
PLL_GND	6	PLL_GND	6
TEST_MODE	7	TEST_MODE	7
SCAN_EN	142	SCAN_EN	142

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